



GPLD94160A

4 x 160-dots Field Sequential LCD Controller / Driver

Aug. 05, 2009

Version 1.0

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4 x 160-dots Field Sequential LCD Controller / Driver

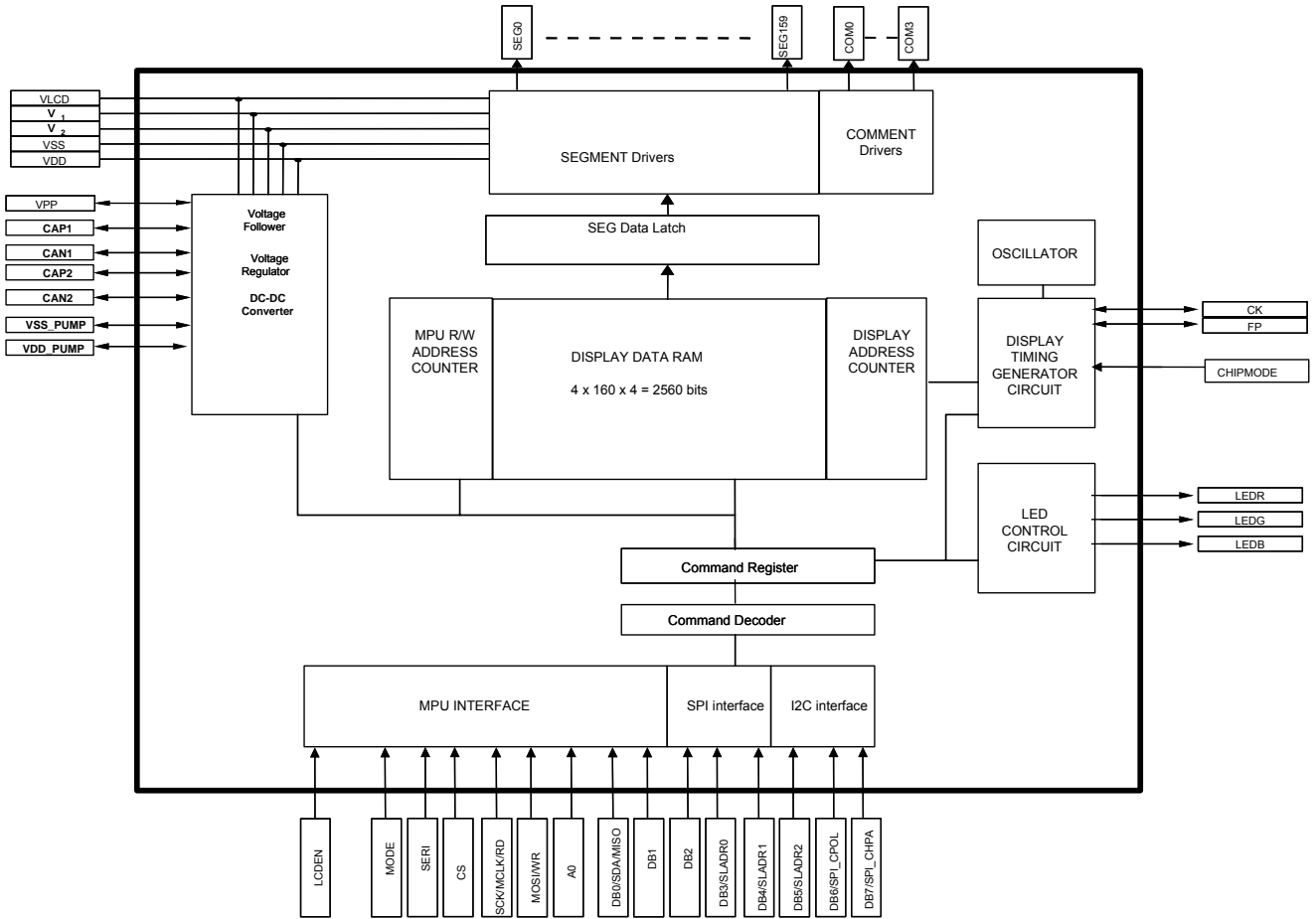
1. GENERAL DESCRIPTION

The GPLD94160A is a Field Sequential LCD controller & driver LSI for graphic dot-matrix liquid crystal display systems. It contains 160 segments and 4 commons driver circuits. This chip is connected directly to a microprocessor, accepts serial peripheral interface (SPI), I²C interface, 68000 and 8080 parallel interface, stores display data in an on-chip display data RAM of 4 x 160 x 4bits. And the capacity of the display can be increased through the use of master/slave multi-chip structures. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, it also can produce LEDR, LEDG, LEDB control signals to generate RGB LED backlight system if necessary. It also features DC/DC converter, voltage regulation and voltage follower to generate LCD driver voltage.

2. FEATURES

- Single-chip LCD Controller & Driver
- Driver Output Circuits: 160 segment / 4 common outputs
- On-chip Display Data Ram
 - Capacity: 160x4x4=2560bits
- Microprocessor Interface
 - 8 bi-directional parallel interface with 8080-series and 68000-series support both read and write modes.
 - SPI serial peripheral interface supports both read and write modes.
 - I²C interface supports both read and write modes.
- On-chip Low Power Analog Circuit
 - Generation of LCD supply voltage (externally VLCD voltage supply is possible)
 - Generation of intermediate LCD bias voltages (1/1, 1/2, 1/3 Bias selectable)
 - Internal Oscillator requires no external components
 - Built-in 2 ~ 3X charge pump
- Logic Supply Voltage Range
 - VDDI (VDD, VDD1)-VSS: 2.4V~3.6V
- LCD Driving Voltage Range (VOP=VLCD-VSS)
 - 3.45 V to 7.2V (Each step: 0.25V)
- Display Function
 - Display ON / OFF
 - Set initial display line
 - Read LED plane status
 - Auto sequential write / read display data
 - Supports COM normal/reverse direction and SEG normal / reverse direction
 - Four color fields selectable for total 16 colors at one picture at most
 - Max. 8 color fields sequence to minimize color breakup effect
 - Supports sequential RAM read, sequential RAM write, and sequential RAM read-modify-write
 - Color field weight adjustable
- With LED Control (LEDR,LEDG,LEDB) pins
 - Max 4mA (active high or active low), four driving strength selectable
- Supports master/slave cascade mode for extend display dots
- SPI interface support 4 mode (Mode0 ~ Mode3) by clock polarity or phase
- Temperature Range : -20 ~75°C
- Package Type :COG

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Mnemonic	PIN No.	Type	Description						
CS	6	I	SPI/Parallel chip enable (Low active)						
LCDEN	5	I	Enable("H")/Disable("L") all LCD output (standby) Also reset input pin When LCDEN is "L", initialization is executed.						
SERI	16	I	SERI : SPI,I ² C / Parallel select 1: serial mode ; 0 : parallel mode						
MODE	17	I	SERI	MODE	Interface mode	Address /Data	Data	Read / Write	Serial clock
			H	H	Serial SPI interface	First byte: address Other byte: data	MOSI (WR) MISO(DB0)	MSB of first byte	MCLK(RD)
			H	L	Serial I ² C interface	I ² C standard	SDA(DB0)	I ² C standard	SCLK(RD)
			L	H	Parallel 8080 interface	A0	DB7 to DB0	RD/E WR/R_W	
			L	L	Parallel 68000 interface	A0	DB7 to DB0	RD/E WR/R_W	
			Mode: 8080 / 6800 for parallel, SPI/I ² C for serial						
RD/E/SCLK/MCLK	3	I	SPI serial clock/ Parallel RD/I ² C SCK/ Parallel 68000 E						
			SERI	MODE	Interface mode	RD/E/SCLK/MCLK	Description		
			H	H	Serial SPI interface	MCLK	SPI clock		
			H	L	Serial I ² C interface	SCLK	I ² C SCK		
			L	H	Parallel 8080 interface	RD	Read enable clock input pin When RD is "L", DB0 to DB7 are in an output status.		
			L	L	Parallel 68000 interface	E	Read / Write control input pin - RW = "H": When E is "H", DB0 to DB7 are in an output status. - RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal.		
WR/R_W/MOSI	2	I	SPI serial data input/ Parallel 8080 WR/ Parallel 68000 R_W						
			SERI	MODE	Interface mode	WR/R_W/MOSI	Description		
			H	H	Serial SPI interface	MOSI	Serial SPI data input		
			H	L	Serial I ² C interface				
			L	H	Parallel 8080 interface	WR	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the WR signal.		
			L	L	Parallel 68000 interface	R_W	Read / Write control input pin - RW = "H": read - RW = "L": write		
A0	4	I	Parallel A0 - A0 = "H": DB0 to DB7 are address						

Mnemonic	PIN No.	Type	Description																																													
			-A0 = "L": DB0 to DB7 are data																																													
DB[7:0]	15-8	I/O	<p>MPU data bus</p> <table border="1"> <thead> <tr> <th>Interface mode</th> <th>Serial SPI interface</th> <th>Serial I²C interface</th> <th>Parallel 8080 interface</th> <th>Parallel 68000 interface</th> </tr> </thead> <tbody> <tr> <td>DB7</td> <td>SPI_CPHA</td> <td>Unconnected</td> <td>DB7</td> <td>DB7</td> </tr> <tr> <td>DB6</td> <td>SPI_CPOL</td> <td>Unconnected</td> <td>DB6</td> <td>DB6</td> </tr> <tr> <td>DB5</td> <td>Unconnected</td> <td>SLADR2</td> <td>DB5</td> <td>DB5</td> </tr> <tr> <td>DB4</td> <td>Unconnected</td> <td>SLADR1</td> <td>DB4</td> <td>DB4</td> </tr> <tr> <td>DB3</td> <td>Unconnected</td> <td>SLADR0</td> <td>DB3</td> <td>DB3</td> </tr> <tr> <td>DB2</td> <td>Unconnected</td> <td>Unconnected</td> <td>DB2</td> <td>DB2</td> </tr> <tr> <td>DB1</td> <td>Unconnected</td> <td>Unconnected</td> <td>DB1</td> <td>DB1</td> </tr> <tr> <td>DB0</td> <td>MISO</td> <td>SDA</td> <td>DB0</td> <td>DB0</td> </tr> </tbody> </table> <p>SPI_CPOL: SPI clock polarity SPI_CPHA: SPI clock phase MISO: SPI data out SLADR[2:0]: I²C slave address option SDA :I²C serial data</p>	Interface mode	Serial SPI interface	Serial I ² C interface	Parallel 8080 interface	Parallel 68000 interface	DB7	SPI_CPHA	Unconnected	DB7	DB7	DB6	SPI_CPOL	Unconnected	DB6	DB6	DB5	Unconnected	SLADR2	DB5	DB5	DB4	Unconnected	SLADR1	DB4	DB4	DB3	Unconnected	SLADR0	DB3	DB3	DB2	Unconnected	Unconnected	DB2	DB2	DB1	Unconnected	Unconnected	DB1	DB1	DB0	MISO	SDA	DB0	DB0
Interface mode	Serial SPI interface	Serial I ² C interface	Parallel 8080 interface	Parallel 68000 interface																																												
DB7	SPI_CPHA	Unconnected	DB7	DB7																																												
DB6	SPI_CPOL	Unconnected	DB6	DB6																																												
DB5	Unconnected	SLADR2	DB5	DB5																																												
DB4	Unconnected	SLADR1	DB4	DB4																																												
DB3	Unconnected	SLADR0	DB3	DB3																																												
DB2	Unconnected	Unconnected	DB2	DB2																																												
DB1	Unconnected	Unconnected	DB1	DB1																																												
DB0	MISO	SDA	DB0	DB0																																												
CHIPMODE	18	I	<p>Master / slave mode select input</p> <p>Master makes some signals for display, and slave gets them. This is for display synchronization.</p> <p>-CHIPMODE = "H": slave mode -CHIPMODE = "L": master mode</p> <p>The following table depends on the CHIPMODE status.</p> <table border="1"> <thead> <tr> <th>CHIPMODE</th> <th>OSC circuit</th> <th>Power supply circuit</th> <th>CK</th> <th>FP</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>Enabled</td> <td>Enabled</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>H</td> <td>Disabled</td> <td>Disabled</td> <td>Input</td> <td>Input</td> </tr> </tbody> </table>	CHIPMODE	OSC circuit	Power supply circuit	CK	FP	L	Enabled	Enabled	Output	Output	H	Disabled	Disabled	Input	Input																														
CHIPMODE	OSC circuit	Power supply circuit	CK	FP																																												
L	Enabled	Enabled	Output	Output																																												
H	Disabled	Disabled	Input	Input																																												
FP	7	I/O	<p>Frame sync.</p> <p>When the GPLD94160A is used in master/slave mode (multi-chip), the FP pins must be connected each other.</p>																																													
CK	1	I/O	<p>Clock sync.</p> <p>When the GPLD94160A is used in master/slave mode (multi-chip), the CK pins must be connected each other.</p>																																													
SEG[0:159]	62-141, 146-225	O	LCD SEG driver output																																													
COML[0:3]	227,226,144, 145	O	LCD common driver output																																													
COMR[0:3]	60,61,143, 142	O	LCD common driver output																																													
LEDR	21,22	O	Red LED control output																																													
LEDG	23,24	O	Green LED control output																																													
LEDB	25,26	O	Blue LED control output																																													
VLCD	38,39	I/O	VLCD power																																													
V1	42,43	I/O	V1 for LCD driver level																																													
V2	40,41	I/O	V2 for LCD driver level																																													
VPP	50,51	P	DC-DC voltage converter output.																																													
CAP1	52,53	P	DC-DC Pump capacitor																																													



GPLD94160A

Mnemonic	PIN No.	Type	Description
CAN1	54,55	P	DC-DC Pump capacitor
CAP2	56,57	P	DC-DC Pump capacitor
CAN2	58,59	P	DC-DC Pump capacitor
VDD_PUMP	44-46	P	VDD for charge pump
VSS_PUMP	47-49	P	VSS for charge pump
VDD	19, 27-31	P	Power
VSS	20, 32-34	P	Ground
IOVSS	35-37	P	SEG/COM ground
TEST0~TEST4	T1~T5		TEST pins and let them open

GPLD94160 recommended I/O PIN ITO Resistance:

PIN Name	ITO Resister
VLCD V1 V2 VPP CAP1 CAN1 CAP2 CAN2 VDD_PUMP VSS_PUMP VDD VSS IOVSS	<100Ω
LEDR LEDG LEDB	<300Ω
CS LCDEN SERI MODE RD WR A0 DB[7:0] CHIPMODE FP CK	<1KΩ

4.1. PAD Assignment

Pin	Symbol	Function	Segment
CK	[Symbol]	CON1	SEG109
WR	[Symbol]	CON1	SEG158
RD	[Symbol]	CON1	SEG157
A0	[Symbol]	CON1	SEG156
LDCEN	[Symbol]	CON1	SEG155
CS	[Symbol]	CON1	SEG154
FP	[Symbol]	CON1	SEG153
DB0	[Symbol]	CON1	SEG152
DB1	[Symbol]	CON1	SEG149
DB2	[Symbol]	CON1	SEG148
DB3	[Symbol]	CON1	SEG147
DB4	[Symbol]	CON1	SEG146
DB5	[Symbol]	CON1	SEG145
DB6	[Symbol]	CON1	SEG144
DB7	[Symbol]	CON1	SEG143
DB8	[Symbol]	CON1	SEG142
DB9	[Symbol]	CON1	SEG141
DB10	[Symbol]	CON1	SEG140
DB11	[Symbol]	CON1	SEG139
DB12	[Symbol]	CON1	SEG138
DB13	[Symbol]	CON1	SEG137
DB14	[Symbol]	CON1	SEG136
DB15	[Symbol]	CON1	SEG135
DB16	[Symbol]	CON1	SEG134
DB17	[Symbol]	CON1	SEG133
DB18	[Symbol]	CON1	SEG132
DB19	[Symbol]	CON1	SEG131
DB20	[Symbol]	CON1	SEG130
DB21	[Symbol]	CON1	SEG129
DB22	[Symbol]	CON1	SEG128
DB23	[Symbol]	CON1	SEG127
DB24	[Symbol]	CON1	SEG126
DB25	[Symbol]	CON1	SEG125
DB26	[Symbol]	CON1	SEG124
DB27	[Symbol]	CON1	SEG123
DB28	[Symbol]	CON1	SEG122
DB29	[Symbol]	CON1	SEG121
DB30	[Symbol]	CON1	SEG120
DB31	[Symbol]	CON1	SEG119
DB32	[Symbol]	CON1	SEG118
DB33	[Symbol]	CON1	SEG117
DB34	[Symbol]	CON1	SEG116
DB35	[Symbol]	CON1	SEG115
DB36	[Symbol]	CON1	SEG114
DB37	[Symbol]	CON1	SEG113
DB38	[Symbol]	CON1	SEG112
DB39	[Symbol]	CON1	SEG111
DB40	[Symbol]	CON1	SEG110
DB41	[Symbol]	CON1	SEG109
DB42	[Symbol]	CON1	SEG108
DB43	[Symbol]	CON1	SEG107
DB44	[Symbol]	CON1	SEG106
DB45	[Symbol]	CON1	SEG105
DB46	[Symbol]	CON1	SEG104
DB47	[Symbol]	CON1	SEG103
DB48	[Symbol]	CON1	SEG102
DB49	[Symbol]	CON1	SEG101
DB50	[Symbol]	CON1	SEG100
DB51	[Symbol]	CON1	SEG99
DB52	[Symbol]	CON1	SEG98
DB53	[Symbol]	CON1	SEG97
DB54	[Symbol]	CON1	SEG96
DB55	[Symbol]	CON1	SEG95
DB56	[Symbol]	CON1	SEG94
DB57	[Symbol]	CON1	SEG93
DB58	[Symbol]	CON1	SEG92
DB59	[Symbol]	CON1	SEG91
DB60	[Symbol]	CON1	SEG90
DB61	[Symbol]	CON1	SEG89
DB62	[Symbol]	CON1	SEG88
DB63	[Symbol]	CON1	SEG87
DB64	[Symbol]	CON1	SEG86
DB65	[Symbol]	CON1	SEG85
DB66	[Symbol]	CON1	SEG84
DB67	[Symbol]	CON1	SEG83
DB68	[Symbol]	CON1	SEG82
DB69	[Symbol]	CON1	SEG81
DB70	[Symbol]	CON1	SEG80
DB71	[Symbol]	CON1	CON6.3
DB72	[Symbol]	CON1	CON6.2
DB73	[Symbol]	CON1	CON6.1
DB74	[Symbol]	CON1	CON6.0
DB75	[Symbol]	CON1	CON5.9
DB76	[Symbol]	CON1	CON5.8
DB77	[Symbol]	CON1	CON5.7
DB78	[Symbol]	CON1	CON5.6
DB79	[Symbol]	CON1	CON5.5
DB80	[Symbol]	CON1	CON5.4
DB81	[Symbol]	CON1	CON5.3
DB82	[Symbol]	CON1	CON5.2
DB83	[Symbol]	CON1	CON5.1
DB84	[Symbol]	CON1	CON5.0
DB85	[Symbol]	CON1	CON4.9
DB86	[Symbol]	CON1	CON4.8
DB87	[Symbol]	CON1	CON4.7
DB88	[Symbol]	CON1	CON4.6
DB89	[Symbol]	CON1	CON4.5
DB90	[Symbol]	CON1	CON4.4
DB91	[Symbol]	CON1	CON4.3
DB92	[Symbol]	CON1	CON4.2
DB93	[Symbol]	CON1	CON4.1
DB94	[Symbol]	CON1	CON4.0
DB95	[Symbol]	CON1	CON3.9
DB96	[Symbol]	CON1	CON3.8
DB97	[Symbol]	CON1	CON3.7
DB98	[Symbol]	CON1	CON3.6
DB99	[Symbol]	CON1	CON3.5
DB100	[Symbol]	CON1	CON3.4
DB101	[Symbol]	CON1	CON3.3
DB102	[Symbol]	CON1	CON3.2
DB103	[Symbol]	CON1	CON3.1
DB104	[Symbol]	CON1	CON3.0
DB105	[Symbol]	CON1	CON2.9
DB106	[Symbol]	CON1	CON2.8
DB107	[Symbol]	CON1	CON2.7
DB108	[Symbol]	CON1	CON2.6
DB109	[Symbol]	CON1	CON2.5
DB110	[Symbol]	CON1	CON2.4
DB111	[Symbol]	CON1	CON2.3
DB112	[Symbol]	CON1	CON2.2
DB113	[Symbol]	CON1	CON2.1
DB114	[Symbol]	CON1	CON2.0
DB115	[Symbol]	CON1	CON1.9
DB116	[Symbol]	CON1	CON1.8
DB117	[Symbol]	CON1	CON1.7
DB118	[Symbol]	CON1	CON1.6
DB119	[Symbol]	CON1	CON1.5
DB120	[Symbol]	CON1	CON1.4
DB121	[Symbol]	CON1	CON1.3
DB122	[Symbol]	CON1	CON1.2
DB123	[Symbol]	CON1	CON1.1
DB124	[Symbol]	CON1	CON1.0
DB125	[Symbol]	CON1	CON0.9
DB126	[Symbol]	CON1	CON0.8
DB127	[Symbol]	CON1	CON0.7
DB128	[Symbol]	CON1	CON0.6
DB129	[Symbol]	CON1	CON0.5
DB130	[Symbol]	CON1	CON0.4
DB131	[Symbol]	CON1	CON0.3
DB132	[Symbol]	CON1	CON0.2
DB133	[Symbol]	CON1	CON0.1
DB134	[Symbol]	CON1	CON0.0
DB135	[Symbol]	CON1	CON0.0
DB136	[Symbol]	CON1	CON0.0
DB137	[Symbol]	CON1	CON0.0
DB138	[Symbol]	CON1	CON0.0
DB139	[Symbol]	CON1	CON0.0
DB140	[Symbol]	CON1	CON0.0
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DB142	[Symbol]	CON1	CON0.0
DB143	[Symbol]	CON1	CON0.0
DB144	[Symbol]	CON1	CON0.0
DB145	[Symbol]	CON1	CON0.0
DB146	[Symbol]	CON1	CON0.0
DB147	[Symbol]	CON1	CON0.0
DB148	[Symbol]	CON1	CON0.0
DB149	[Symbol]	CON1	CON0.0
DB150	[Symbol]	CON1	CON0.0
DB151	[Symbol]	CON1	CON0.0
DB152	[Symbol]	CON1	CON0.0
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DB154	[Symbol]	CON1	CON0.0
DB155	[Symbol]	CON1	CON0.0
DB156	[Symbol]	CON1	CON0.0
DB157	[Symbol]	CON1	CON0.0
DB158	[Symbol]	CON1	CON0.0
DB159	[Symbol]	CON1	CON0.0
DB160	[Symbol]	CON1	CON0.0
DB161	[Symbol]	CON1	CON0.0
DB162	[Symbol]	CON1	CON0.0
DB163	[Symbol]	CON1	CON0.0
DB164	[Symbol]	CON1	CON0.0
DB165	[Symbol]	CON1	CON0.0
DB166	[Symbol]	CON1	CON0.0
DB167	[Symbol]	CON1	CON0.0
DB168	[Symbol]	CON1	CON0.0
DB169	[Symbol]	CON1	CON0.0
DB170	[Symbol]	CON1	CON0.0
DB171	[Symbol]	CON1	CON0.0
DB172	[Symbol]	CON1	CON0.0
DB173	[Symbol]	CON1	CON0.0
DB174	[Symbol]	CON1	CON0.0
DB175	[Symbol]	CON1	CON0.0
DB176	[Symbol]	CON1	CON0.0
DB177	[Symbol]	CON1	CON0.0
DB178	[Symbol]	CON1	CON0.0
DB179	[Symbol]	CON1	CON0.0
DB180	[Symbol]	CON1	CON0.0
DB181	[Symbol]	CON1	CON0.0
DB182	[Symbol]	CON1	CON0.0
DB183	[Symbol]	CON1	CON0.0
DB184	[Symbol]	CON1	CON0.0
DB185	[Symbol]	CON1	CON0.0
DB186	[Symbol]	CON1	CON0.0
DB187	[Symbol]	CON1	CON0.0
DB188	[Symbol]	CON1	CON0.0
DB189	[Symbol]	CON1	CON0.0
DB190	[Symbol]	CON1	CON0.0
DB191	[Symbol]	CON1	CON0.0
DB192	[Symbol]	CON1	CON0.0
DB193	[Symbol]	CON1	CON0.0
DB194	[Symbol]	CON1	CON0.0
DB195	[Symbol]	CON1	CON0.0
DB196	[Symbol]	CON1	CON0.0
DB197	[Symbol]	CON1	CON0.0
DB198	[Symbol]	CON1	CON0.0
DB199	[Symbol]	CON1	CON0.0
DB200	[Symbol]	CON1	CON0.0

The IC substrate should be connected to VSS or floating

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1F capacitor between VDD and VSS should be placed to IC as close as possible.

5. FUNCTIONAL DESCRIPTIONS

5.1. Microprocessor Interface

5.1.1. Chip Select Input

There is a CS pin for chip selection. The GPLD94160A can communicate with an MPU when CS is "L". When CS is "H", the internal shift register and the counters are reset.

5.1.2. Selecting Parallel / Serial interface

GPLD94160A has four types of interfaces with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by SERI and MODE pins.

Parallel / Serial Interface Mode

SERI	H	H	L	L
MODE	H	L	H	L
Interface mode	Serial SPI interface	Serial I2C interface	Parallel 8080 interface	Parallel 68000 interface
A0	Unconnected	Unconnected	A0	A0
CS	CS	Unconnected	CS	CS
RD/E/SCLK/MCLK	MCLK	SCLK	RD	E
WR/R_W/MOSI	MOSI	Unconnected	WR	R_W
DB7	SPI_CPOL	Unconnected	DB7	DB7
DB6	SPI_CPHA	Unconnected	DB6	DB6
DB5	Unconnected	SLADR[2]	DB5	DB5
DB4	Unconnected	SLADR[1]	DB4	DB4
DB3	Unconnected	SLADR[0]	DB3	DB3
DB2	Unconnected	Unconnected	DB2	DB2
DB1	Unconnected	Unconnected	DB1	DB1
DB0	MISO	SDA	DB0	DB0

5.1.2.1. Parallel interface (6800 and 8080 interface)

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by SERI and MODE as shown in the above table. The type of data transfer is determined by signals at A0, RD/E and WR.R_W as shown in the below table.

Parallel Data Transfer

Common	6800-series		8080-series		Description
	A0	RD/E (E)	WR/R_W (R_W)	RD/E (RD)	
H	H	L	H	L	Address write
L	H	H	L	H	Data read
L	H	L	H	L	Data write

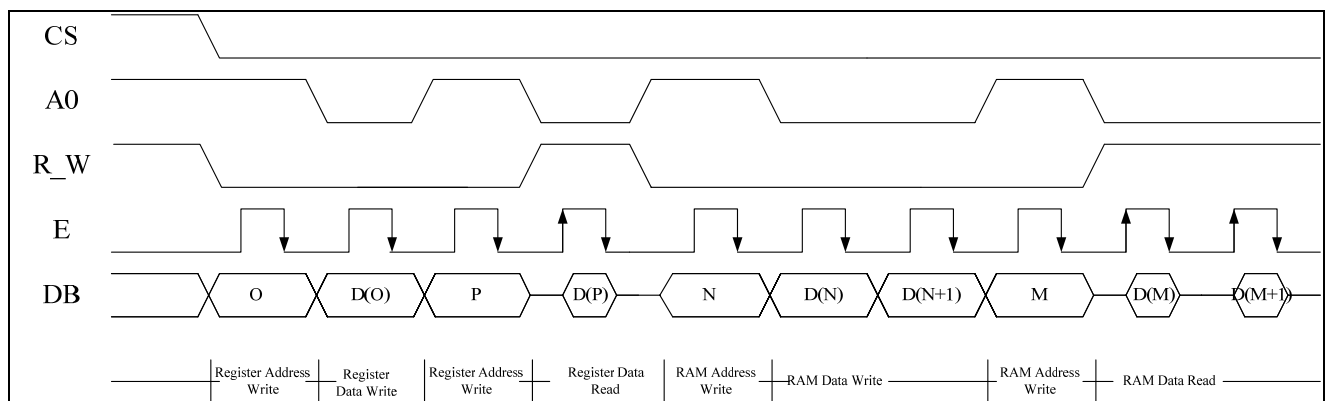


Figure 2: 6800-Series MPU Interface protocol (SERI="L", MODE="L")

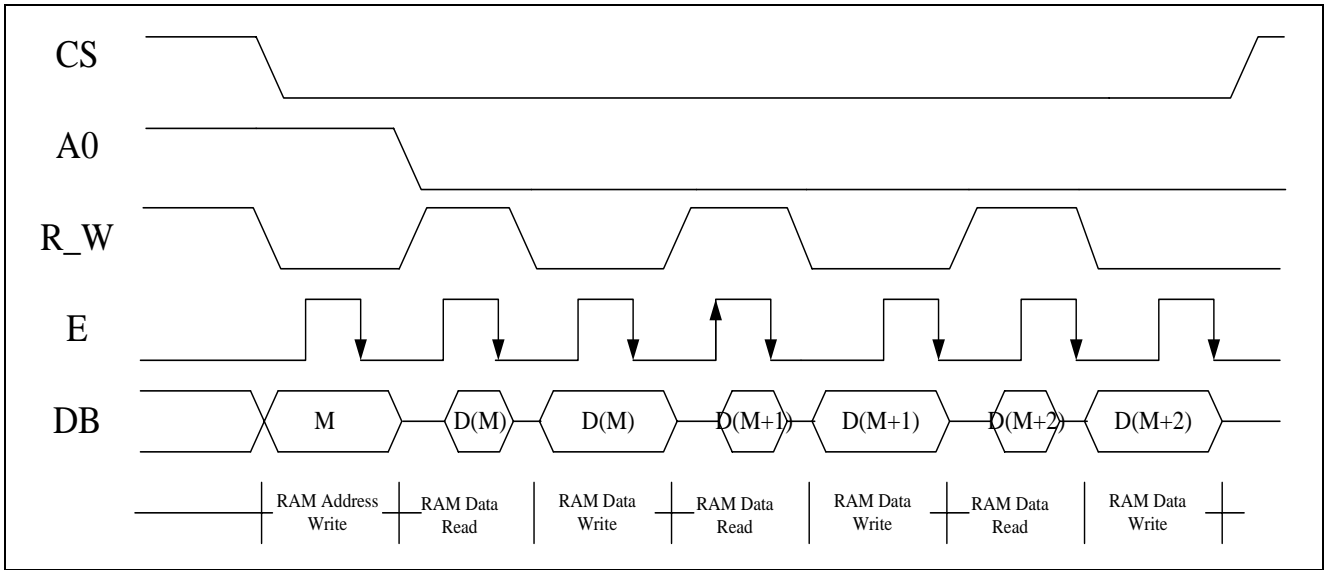


Figure 3: 6800-Series MPU Interface protocol (Read-Modify-Mode)

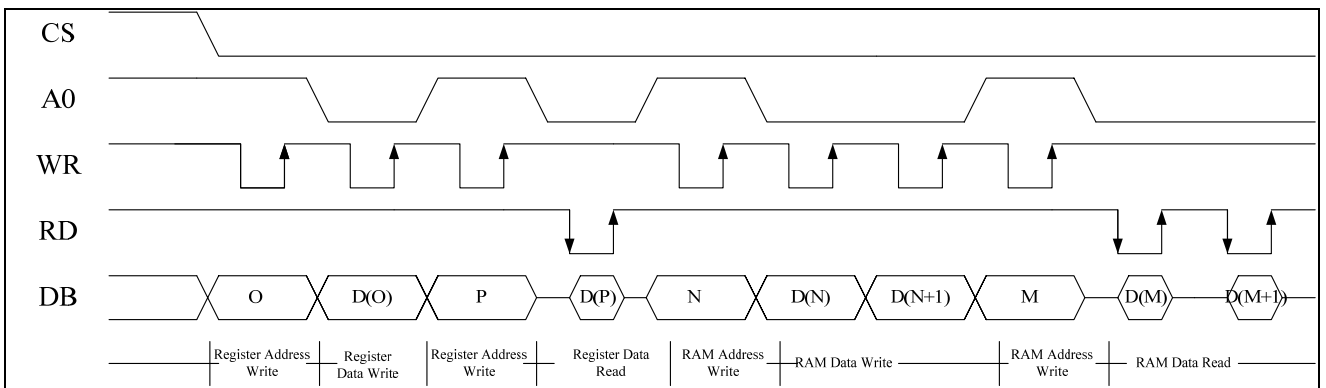


Figure 4: 8080-Series MPU Interface protocol (SERI="L", MODE="H")

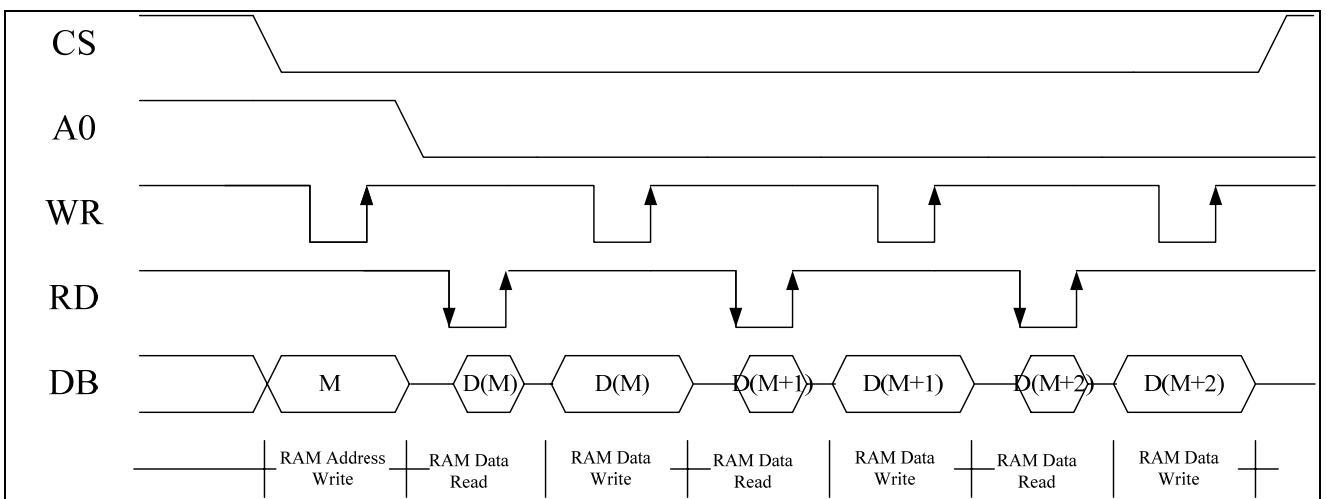


Figure 5: 8080-Series MPU Interface protocol (Read-Modify-Mode)

5.1.2.2. Serial Interface (SPI Interface)

A Serial Peripheral Interface (SPI) interface is supported in GPLD94160. There are four control signals on SPI including CS, MCLK (SCK), MOSI (SDI), and MISO (SDO). Four types of operation mode are configured by two pins, SPI_CPOL and SPI_CPHA. They are supported as follows:

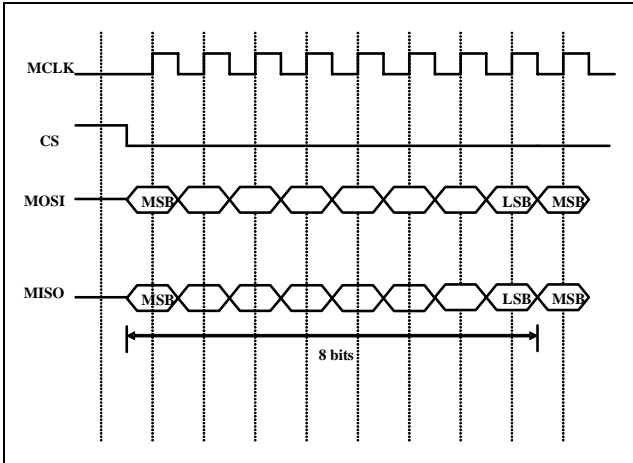


Figure 6: Mode 0 SPI_CPOL=0, SPI_CPHA=0;

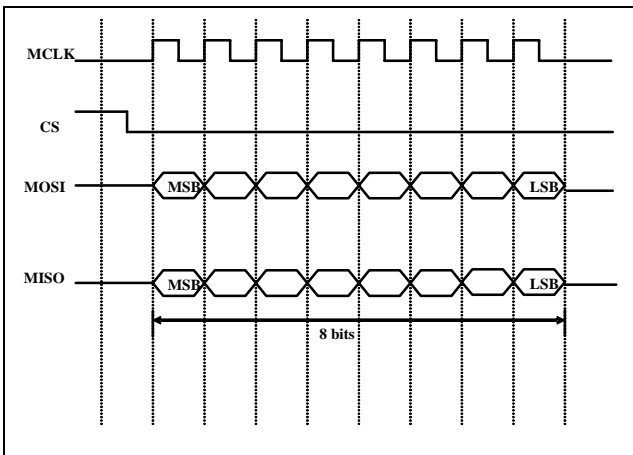


Figure 7: Mode 1 SPI_CPOL=0, SPI_CPHA=1;

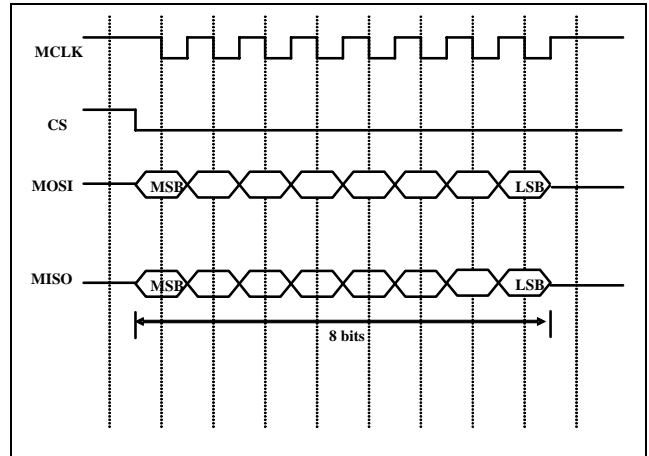


Figure 8: Mode 2 SPI_CPOL=1, SPI_CPHA=0;

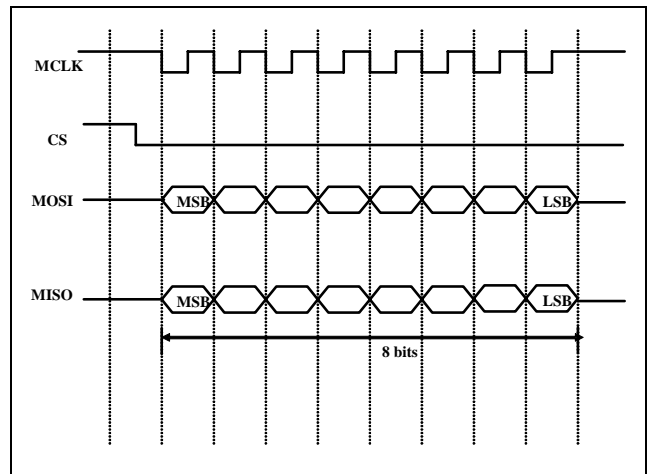


Figure 9: Mode 3 SPI_CPOL=1, SPI_CPHA=1;

The first byte of SPI data received after CS goes low is the register/RAM address users may write. The data transfer of SPI is shown as the below:

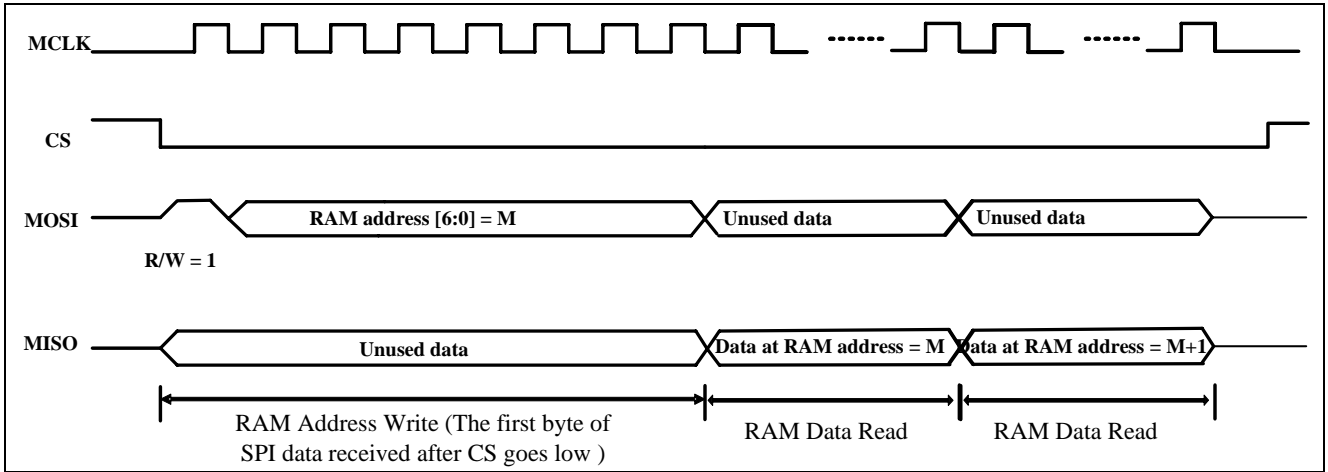


Figure 10: SPI Interface protocol (RAM address write & RAM data read)

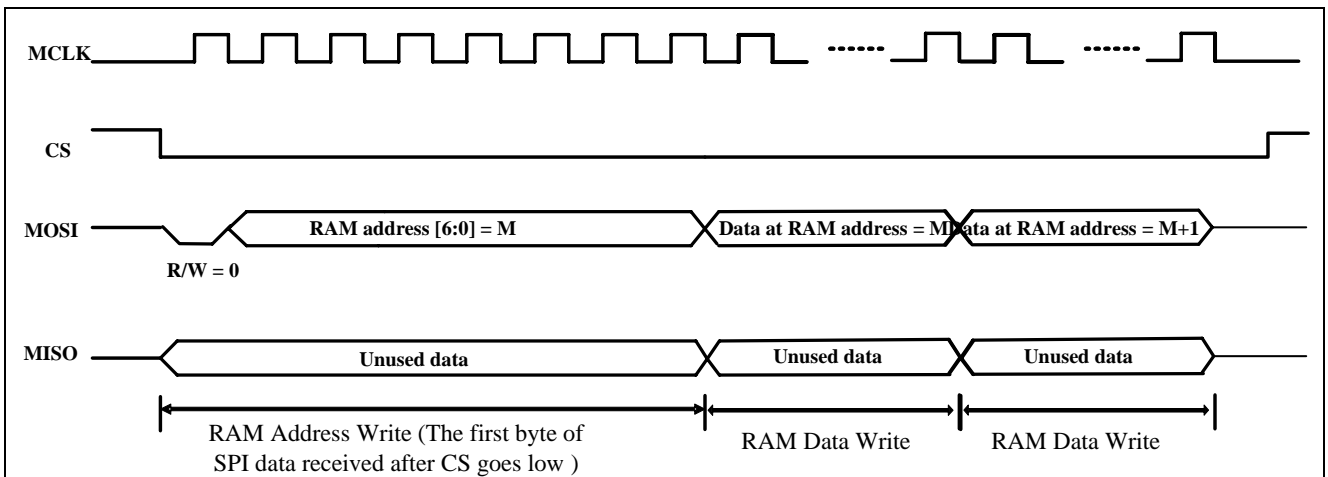


Figure 11: SPI Interface protocol (RAM address write & RAM data write)

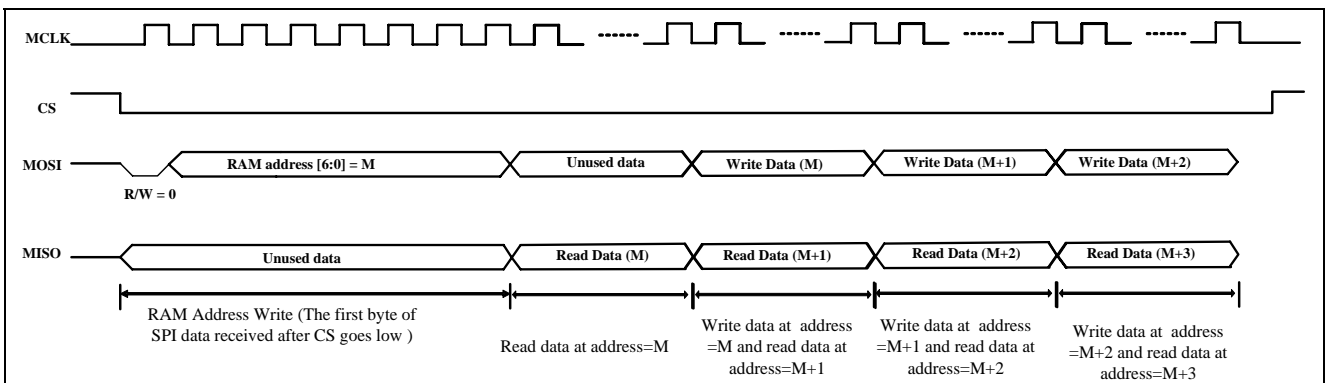


Figure 12: SPI Interface protocol (RAM Read-Modify-Write)

5.1.2.3. Serial Interface (I²C Interface)

A Serial Inter-IC bus Interface (I²C) is supported in GPLD94160. Only two wires (SCK and SDA) need to implement the protocol.

The GPLD94160 uses three device address bits SLADR2 (DB5), SLADR1 (DB4), SLADR0 (DB3) to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The data transfer of I²C is shown as the below:

- = master writes to slave.
- = slave writes to master

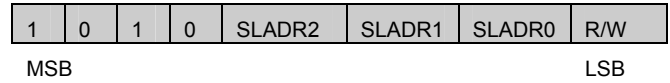


Figure 13: Device Address

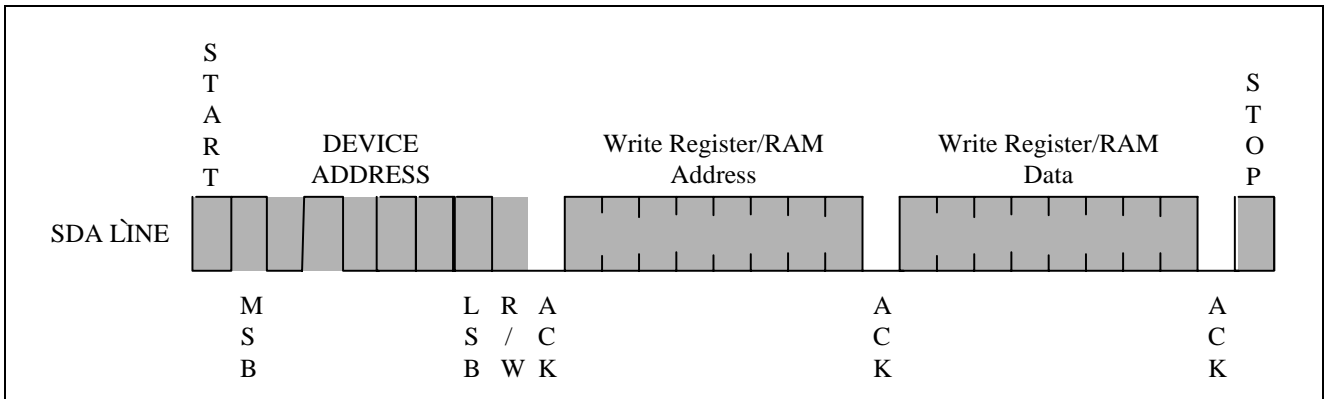


Figure 14: Write Register/RAM data

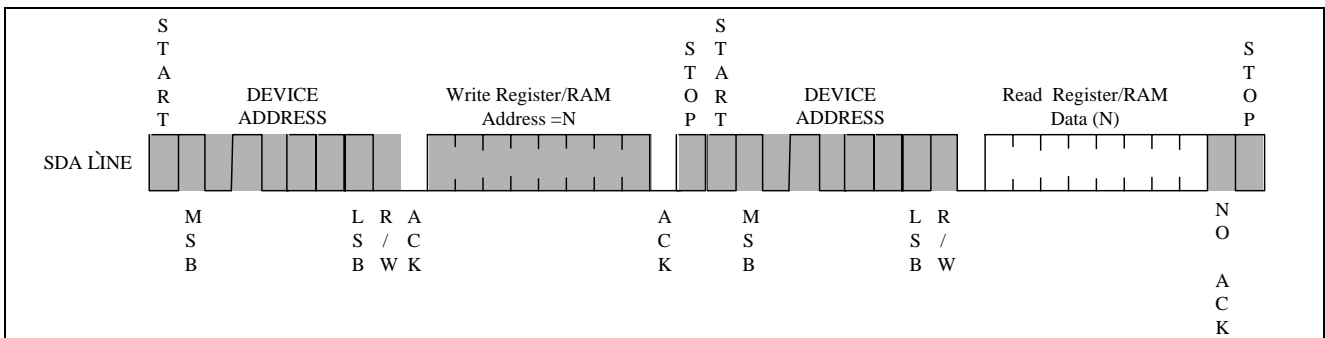


Figure 15: Read Register/RAM data

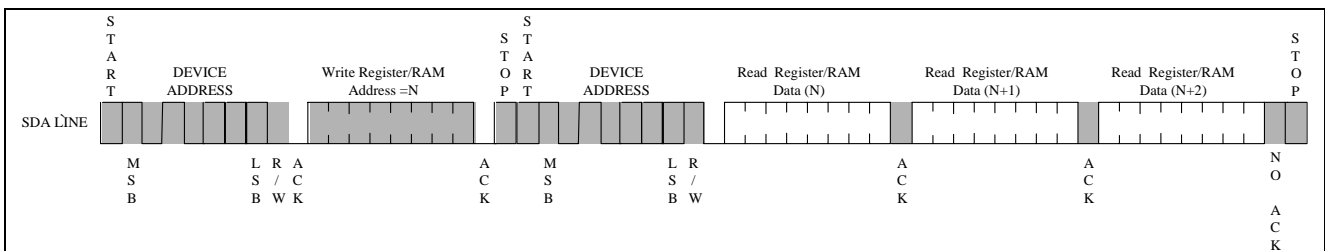


Figure 16: Read Sequential RAM data

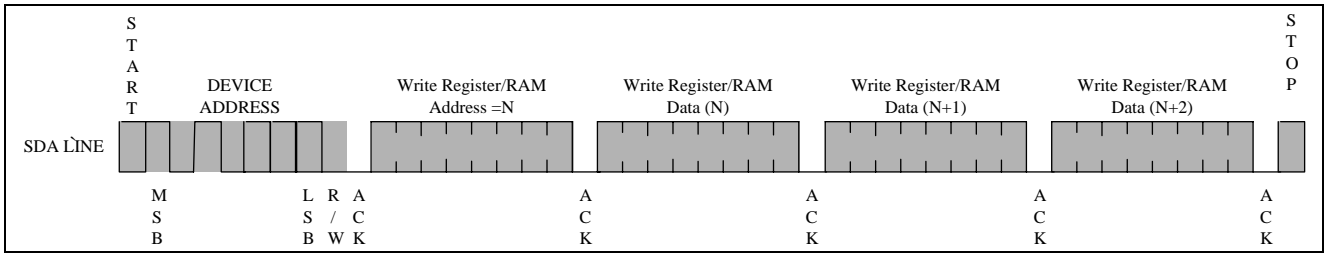


Figure 17: Write Sequential RAM data

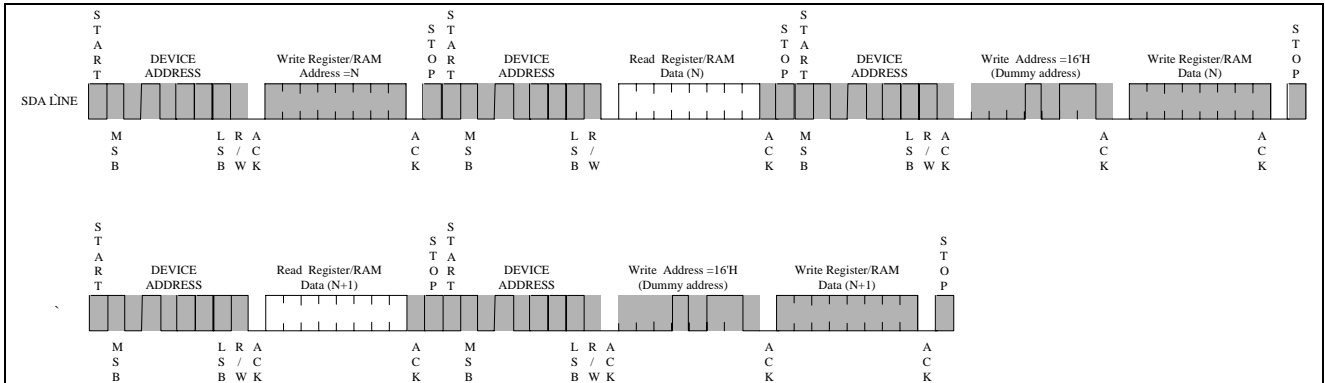


Figure 18: Read-Modify-Write RAM data

5.2. Display Data RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It has 4 x 4 x 160 bits. Each pixel can be selected when the line, field and register addresses are specified. The display data of LCD address mapping correspond to the LCD common lines as shown

in the below. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

COMRSEQ=0; COM display start line(1A'H) = 01'H				COMR3	COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2
COMRSEQ=0; COM display start line(1A'H) = 00'H				COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2	COMR3	COMR0	COMR1	COMR2	COMR3
COMLSEQ=1; COM display start line(1A'H) = 00'H				COML3	COML2	COML1	COML0	COML3	COML2	COML1	COML0	COML3	COML2	COML1	COML0	COML3	COML2	COML1	COML0
COMLSEQ=1; COM display start line(1A'H) = 02'H				COML1	COML0	COML3	COML2	COML1	COML0	COML3	COML2	COML1	COML0	COML3	COML2	COML1	COML0	COML3	COML2
Field address				00H (Color field 0)				01H (Color field 1)				02H (Color field 2)				03H (Color field 3)			
Line address																			
(SEGORD = 0)		(SEGORD = 1)																	
Register (SEG) address	data	Register address	data	00H	01H	02H	03H	00H	01H	02H	03H	00H	01H	02H	03H	00H	01H	02H	03H
20H	B0	33H	B7																
	B1		B6																
	B2		B5																
	B3		B4																
	B4		B3																
	B5		B2																
	B6		B1																
	B7		B0																
21H	B0	32H	B7																
	B1		B6																
	B2		B5																
	B3		B4																
	B4		B3																
	B5		B2																
	B6		B1																
	B7		B0																
⋮	⋮	⋮	⋮																
33H	B0	20H	B7																
	B1		B6																
	B2		B5																
	B3		B4																
	B4		B3																
	B5		B2																
	B6		B1																
	B7		B0																
Register (SEG) address	data	Register address	data																
(SEGORD = 0)		(SEGORD = 1)																	

Figure 19: DDRAM map

5.2.1. DDRAM address

DDRAM addresses consist of field address, line address, and register address. The display data of LCD address mapping is as the above. Field start address can be changed by writing field start address register (1E'H). Line start address can be changed by writing line start address register (18'H). And when register address is within 20'H and 33'H, LCD RAM is actually accessed or written.

5.2.1.1. DDRAM sequential read/write

GPLD94160 supports sequential DDRAM read and write in all interfaces, 6800, 8080, SPI, and I²C in pixel mode and color field mode. Before DDRAM is read or written, field start/end address, line start/end address, and SEG start/end address should be set. Field start/end address value depends on how many color fields

are chosen. Line start/end address value is determined by the number of commons on LCD panel and SEG start/end address value by the number of segments on LCD panel. If not all commons are used, double buffer can be easily achieved by changing COM display start line (1A'H).

Color Field mode

In color field mode (RGB=1), the sequential order of RAM address is SEG, line, and then color field. When field start address (1E'H) is set as 01'H, field end address (1F'H) is 03'H; line start address (18'H) is 00'H; line end address (19'H) is 02'H, and SEG start address (1C'H) is 20'H, SEG end address (1D'H) 30'H, RAM address sequence is as follows:

SEG address	20'H	21'H	30'H	20'H	21'H	...	30'H	20'H	...	30'H	20'H	...	30'H	20'H	...	30'H	20'H	...	30'H
Line address	00'H				01'H				02'H				00'H	...	02'H	00'H	...	00'H	...	00'H
Color field address	01'H								02'H				03'H	01'H	...	02'H				

Figure 20: Color Field mode DDRAM sequential address

Pixel mode:

In pixel mode (RGB=0), RAM address is sequential in color field, SEG, and then line order. When field start address (1E'H) is set as 01'H; field end address (1F'H) is 03'H; line start address (18'H)

is 00'H; line end address (19'H) is 02'H, and SEG start address (1C'H) is 20'H, SEG end address (1D'H) 30'H. RAM address sequence is as follows:

SEG address	20'H		21'H			30'H		20'H			20'H				
Line address	00'H								01'H				02'H				00'H			
Color field address	01'H	02'H	03'H	01'H	02'H	03'H	01'H	02'H	03'H	01'H	02'H	01'H				

Figure 21: Pixel mode DDRAM sequential address

5.3. Booster Circuits

Using the booster voltage circuits equipped within the GPLD94160A chips, it is possible to produce 2X/3X step-up of the (VDD-VSS) voltage levels.

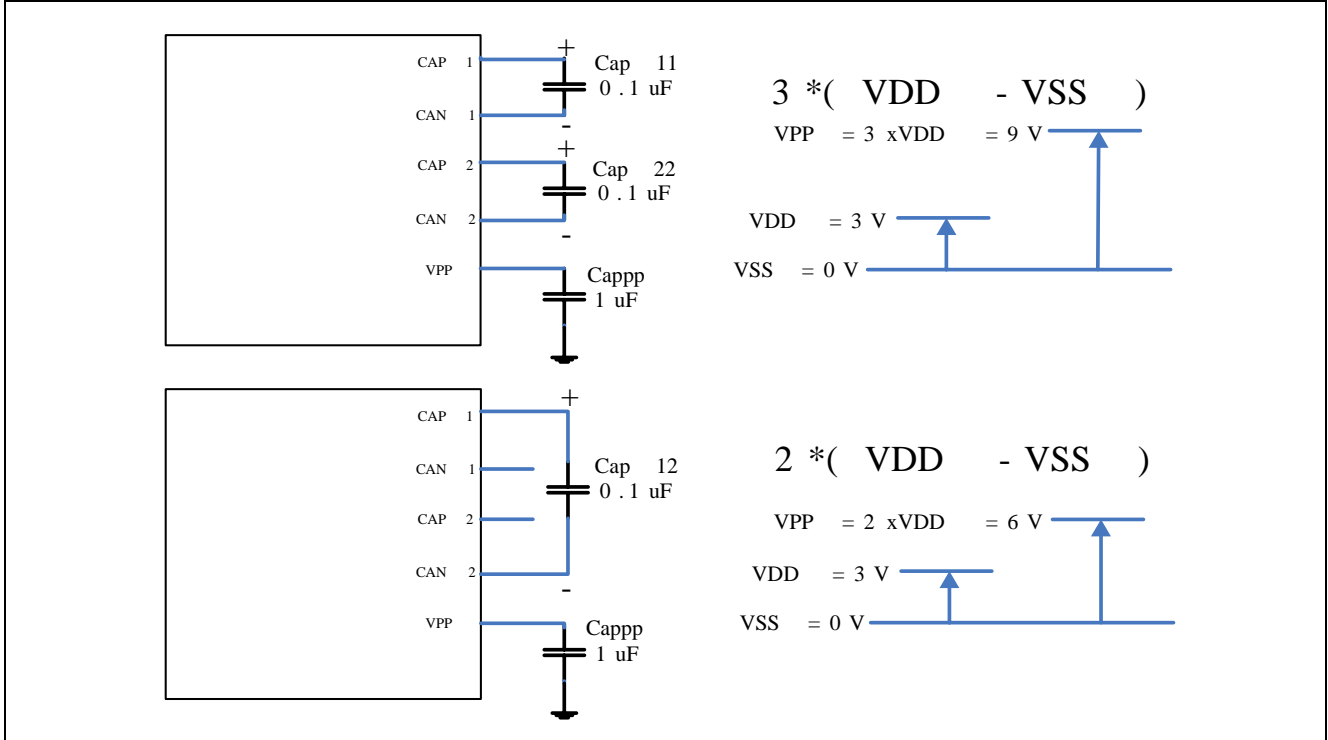


Figure 21: Charge pump

Note: The capacitors value is 0.1uF for cap11, cap22 and cap12.

The capacitors value is 1uF for cappp.

The best ratio of the value of Cappp to Cap11, Cap22 is 10: 1.

Vpp will be clamped about 8.0V

5.4. Regulator Circuits

The pump circuit will pump the voltage up to V_{PP} , which further generates VLCD voltage, VLCD, for the power of voltage regulator circuit.

The VLCD voltage can be controlled by commands alone over the range where $|VLCD| < |VPP|-1V$.

The following table shows the value based on the electronic volume register settings.

VLCDE[3:0]	0000	0001	0010	0011	0100	0101	0110	0111
VLCD	3.45	3.7	3.95	4.2	4.45	4.7	4.95	5.2
VLCDE[3:0]	1000	1001	1010	1011	1100	1101	1110	1111
VLCD	5.45	5.7	5.95	6.2	6.45	6.7	6.95	7.2

5.5. LCD Display Circuits

5.5.1. Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of VDD. The oscillator circuit is only enabled when CHIPMODE = "L" (Master Mode) and OSC_EN = "1" (03'H.B0). In slave mode (CHIPMODE = "H"), CK pin will be input connected to master chip's CK pin.

5.5.2. Display Timing Generator Circuit

This circuit generates some signals for the use of displaying LCD and LED.

5.5.2.1. Composition of one LCD frame

One LCD frame is composed of eight color fields (planes) at most. Four color field settings are available. The interval of each color field is adjustable by setting LCDTx (06'H ~ 09'H). Also, the LED turned on in each color field is adjustable by setting {Bx, Gx, Rx}. For example, it can be set field 0 as red LED on (R0=1), field 1 as green LED on (G1=1), field 2 as blue LED on (B2=1), and field 3 as red and green LED on (R3=1, G3=1). And max plane is set as

"5" (MXFLD = 4'H). And it is set Plane0 as field0, Plane1 as field1, Plane2 as field2, Plane3 as field3, and Plane4 as field2. And LED plane sequence will be R-G-B-RG-B and then R-G-B-RG-B. Different color field sequence is easily achieved to minimize color breakup effect.

$$\text{Frame rate} = 1 / (1 / \text{Fplane}_0 + 1 / \text{Fplane}_1 + \dots + 1 / \text{Fplane}_{\text{max}})$$

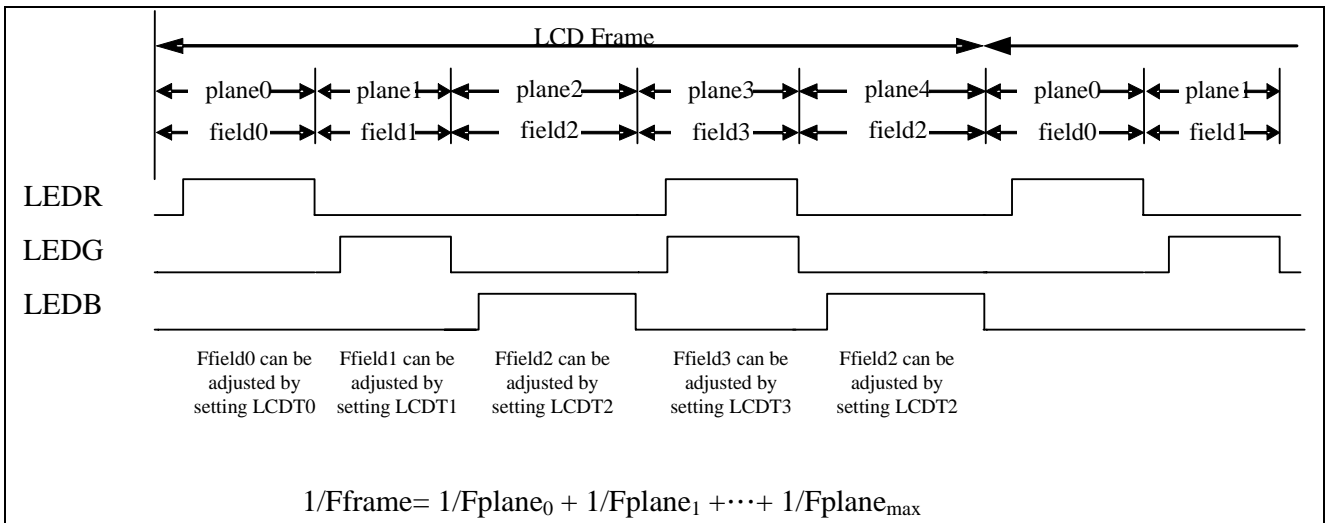


Figure 22: Composition of one LCD frame

Max plane = 5 (MXFLD = 04'H); plane0 = field0, plane1 = field1, plane2 = field2, plane3 = field3, plane4 = field2.

5.5.2.2. Composition of one color field

One color field is composed of two parts: LED part and LCD part.

In LED part, LED delay is adjustable by setting LEDT (0A'H). During LED delay period, red, green and blue LEDs can be all off or all on by setting LEDW (0F'H.B2), which can minimize color breakup effect.

In LCD part, blanking time is adjustable by setting BLT (05'H). During blanking period, the voltage between common and segment can be "0" or "VLCD" by setting BLPOL (05'H.B7). Four to one COM is selectable by setting DUTY (02'H). An AC toggle means a group. The number of group in a color field is adjustable by setting GM (02'H).

The frequency of common in FIELDx = 120KHZ/(OSCT+1)/(LCDTx + 16) .

The period of FIELDx = (1/Fcomx)*(DUTY+1)*(GM+1)*2 + BLT*0.1 ms

It is illustrated as below.

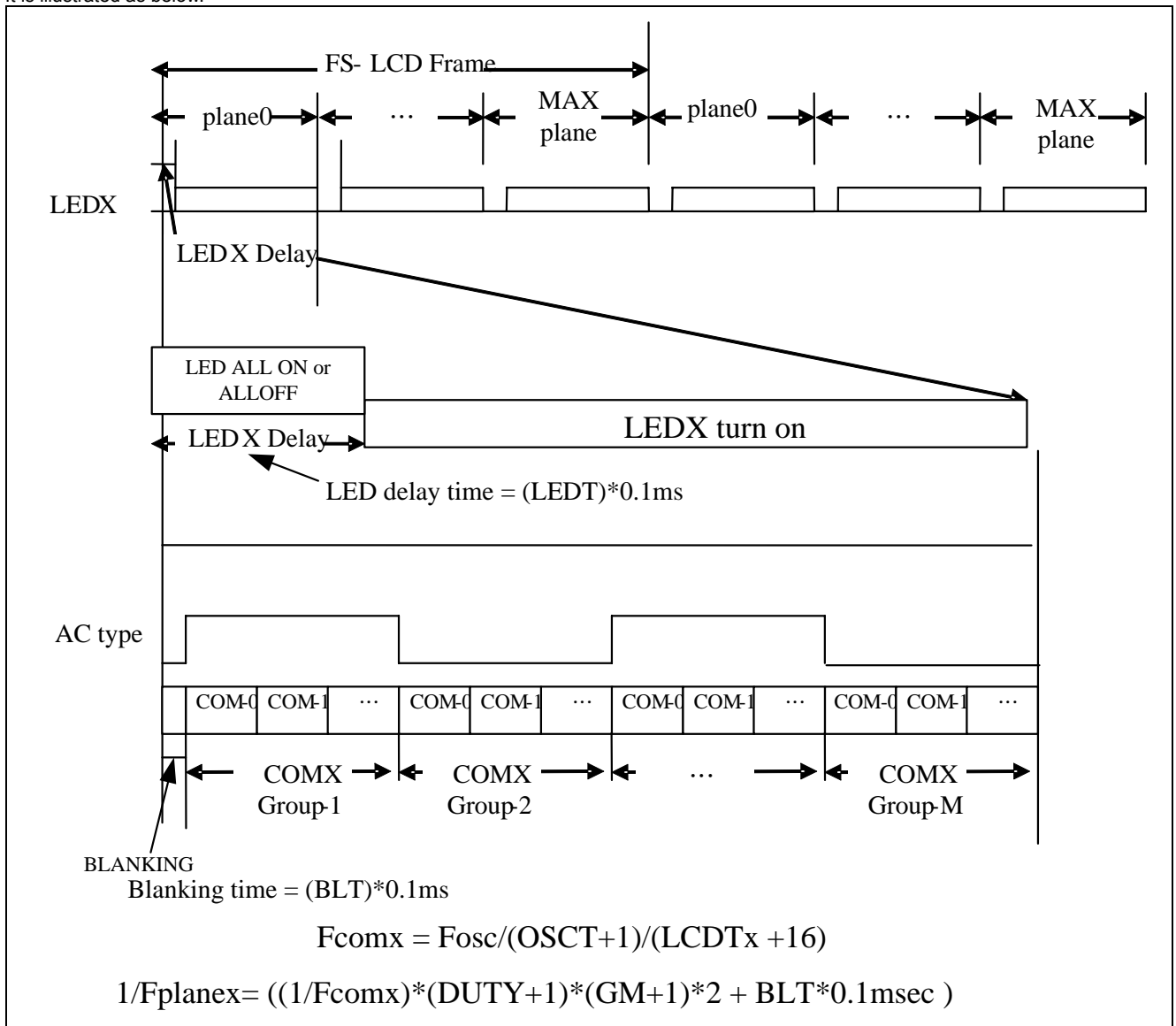


Figure 23: Composition of one color field

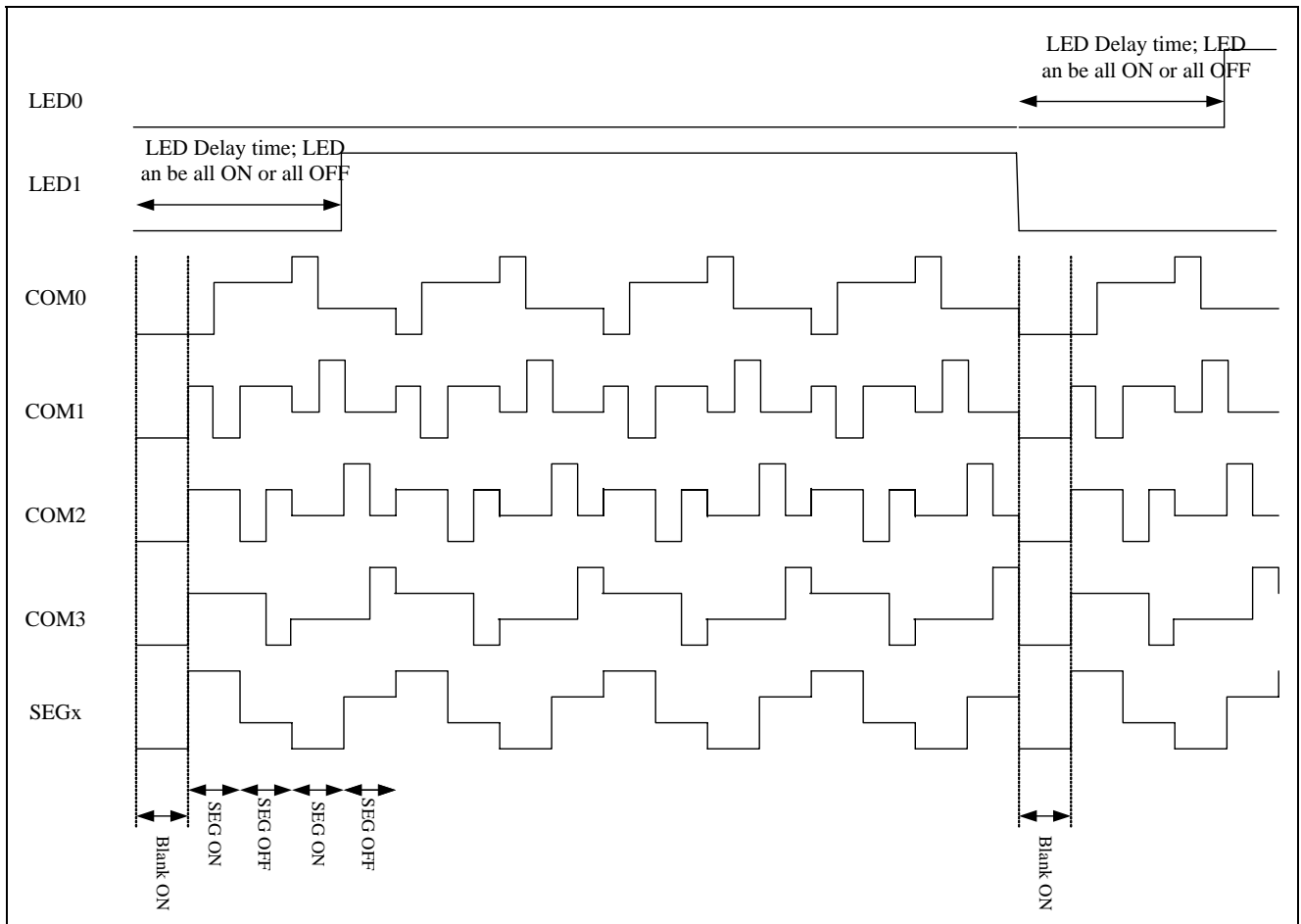


Figure 24: Example of one color field, 4 COM, 1/3 bias, 4 groups

6. COMMAND DESCRIPTION

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value	Read/Write	
00H	NOP	NOP										
01H	LCD Setup1	BIAS	0	SEGORD	0	VLCDE3	VLCDE 2	VLCDE 1	VLCDE 0	0000_0000	W	
02H	LCD Setup2	COM_SPL	0	LCD_EN1	LCD_EN0	GM1	GM0	DUTY1	DUTY0	0000_0000	W	
03H	LCD Setup3	0	0	PKSEL1	PKSEL0	0	CP_ON	OP_ON	OSC_ON	0000_0000	W	
04H	OSC TIME BASE	0	0	0	0	0	OSCT2	OSCT1	OSCT0	0000_0000	W	
05H	Blank Time	BLPOL	COMRSEQ	COMLSEQ	BLT4	BLT3	BLT2	BLT1	BLT0	0000_0000	W	
06H	LCD Time Base0	0	0	0	LCDT04	LCDT03	LCDT02	LCDT01	LCDT00	0000_0000	W	
07H	LCD Time Base1	0	0	0	LCDT14	LCDT13	LCDT12	LCDT11	LCDT10	0000_0000	W	
08H	LCD Time Base2	0	0	0	LCDT24	LCDT23	LCDT22	LCDT21	LCDT20	0000_0000	W	
09H	LCD Time Base3	0	0	0	LCDT34	LCDT33	LCDT32	LCDT31	LCDT30	0000_0000	W	
0AH	LED Setup1	0	0	LEDT5	LEDT4	LEDT3	LEDT2	LEDT1	LEDT0	0000_0000	W	
0BH	Field Setup0	ALLON0	ALLOFF0	0	0	0	B0	G0	R0	0000_0000	W	
0CH	Field Setup1	ALLON1	ALLOFF1	0	0	0	B1	G1	R1	0000_0000	W	
0DH	Field Setup2	ALLON2	ALLOFF2	0	0	0	B2	G2	R2	0000_0000	W	
0EH	Field Setup3	ALLON3	ALLOFF3	0	0	0	B3	G3	R3	0000_0000	W	
0FH	LED Setup2	LED_EN	LED_POL	0	0	0	LEDW	DRVSEL1	DRVSEL0	0000_0000	W	
10H	LED status	0	0	0	0	0	0	LEDS(R)	LEDS(R)		R	
11H		Unused										
12H		Unused										
13H	Software reset	Write A5'H to implement Soft reset										W
14H	MAX Field number	0	0	0	0	0	MXFLD2	MXFLD1	MXFLD0	0000_0000	W	
15H	Field control	0	FLDNM2	FLDNM1	FLDNM 0	0	0	FLDSEL1	FLDSEL0	xxxx_xxxx	W	
16H	RAM dummy address											W
17H	RAM control	0	0	0	0	0	0	RMW	RGB	0000_0000	W	
18H	Line data start address	0	0	0	0	0	0	LNSADR1	LNSADR0	0000_0000	R/W	
19H	Line data end address	0	0	0	0	0	0	LNEADR1	LNEADR0	0000_0011	R/W	
1AH	COM display data start line	0	0	0	0	0	0	CDSLIN1	CDSLIN0	0000_0000	R/W	
1BH		Unused										
1CH	SEG data start address	0	0	1	SSADR4	SSADR3	SSADR2	SSADR1	SSADR0	0010_0000	R/W	
1DH	SEG data end address	0	0	1	SEADR4	SEADR3	SEADR2	SEADR1	SEADR0	0011_1111	R/W	
1EH	Color field start address	0	0	0	0	0	0	FDSADR1	FDSADR0	0000_0000	R/W	
1FH	Color field end address	0	0	0	0	0	0	FDEADR1	FDEADR0	0000_0011	R/W	
20H~33H	RAM data (SEG data)	RAM data (SEG data)								xxxx_xxxx	R/W	

6.1.1. LCD Setup1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
01H	LCD Setup1	BIAS	0	SEGORD	0	VLCDE3	VLCDE 2	VLCDE 1	VLCDE 0	0000_0000

Bit	Function	Type	Description	Condition
7	BIAS	W	LCD bias	0= 1/2 bias 1= 1/3 bias When DUTY=00'B (1 COM), LCD waveform is static in spite of this bit.
6	-	-	Reserved.	
5	SEGORD	W	Define SEG order. When SEGORD = 1, RAM data (20'H ~ 33'H) will map to SEG159 to SEG0. When SEGORD = 0, RAM data (20'H ~ 33'H) will map to SEG0 to SEG159. Please refer to 5.2.DISPLAY DATA RAM (DDRAM) figure (Figure 19).	0= SEG normal order 1= SEG reverse order
4	-	-	Reserved.	
[3:0]	VLCDE	W	LCD VLCD voltage	See the table below

VLCDE3	VLCDE2	VLCDE1	VLCDE0	VLCD
0	0	0	0	3.45
0	0	0	1	3.7
0	0	1	0	3.95
0	0	1	1	4.2
0	1	0	0	4.45
0	1	0	1	4.7
0	1	1	0	4.95
0	1	1	1	5.2
1	0	0	0	5.45
1	0	0	1	5.7
1	0	1	0	5.95
1	0	1	1	6.2
1	1	0	0	6.45
1	1	0	1	6.7
1	1	1	0	6.95
1	1	1	1	7.2

6.1.2. LCD Setup2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
02H	LCD Setup2	COM_SPL	0	LCD_EN1	LCD_EN0	GM1	GM0	DUTY1	DUTY0	0000_0000

Bit	Function	Type	Description	Condition															
7	COM_SPL	W	See the below figure 25																
6	-	-	Reserved.																
[5:4]	LCD_EN	W	LCD_EN	<table border="1"> <thead> <tr> <th colspan="2">LCD_EN</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>LCD all off</td> </tr> <tr> <td>0</td> <td>1</td> <td>LCD all on</td> </tr> <tr> <td>1</td> <td>0</td> <td>LCD enabled, normal display</td> </tr> <tr> <td>1</td> <td>1</td> <td>LCD enabled, inverse display</td> </tr> </tbody> </table>	LCD_EN		Function	0	0	LCD all off	0	1	LCD all on	1	0	LCD enabled, normal display	1	1	LCD enabled, inverse display
LCD_EN		Function																	
0	0	LCD all off																	
0	1	LCD all on																	
1	0	LCD enabled, normal display																	
1	1	LCD enabled, inverse display																	
[3:2]	GM	W	Group Number	<table border="1"> <thead> <tr> <th colspan="2">GM</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Group Number = 2</td> </tr> <tr> <td>0</td> <td>1</td> <td>Group Number = 4</td> </tr> <tr> <td>1</td> <td>0</td> <td>Group Number = 6</td> </tr> <tr> <td>1</td> <td>1</td> <td>Group Number = 8</td> </tr> </tbody> </table>	GM		Function	0	0	Group Number = 2	0	1	Group Number = 4	1	0	Group Number = 6	1	1	Group Number = 8
GM		Function																	
0	0	Group Number = 2																	
0	1	Group Number = 4																	
1	0	Group Number = 6																	
1	1	Group Number = 8																	
[1:0]	DUTY	W	LCD duty	<table border="1"> <thead> <tr> <th colspan="2">DUTY</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 COM</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 COM</td> </tr> <tr> <td>1</td> <td>0</td> <td>3 COM</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 COM</td> </tr> </tbody> </table>	DUTY		Function	0	0	1 COM	0	1	2 COM	1	0	3 COM	1	1	4 COM
DUTY		Function																	
0	0	1 COM																	
0	1	2 COM																	
1	0	3 COM																	
1	1	4 COM																	

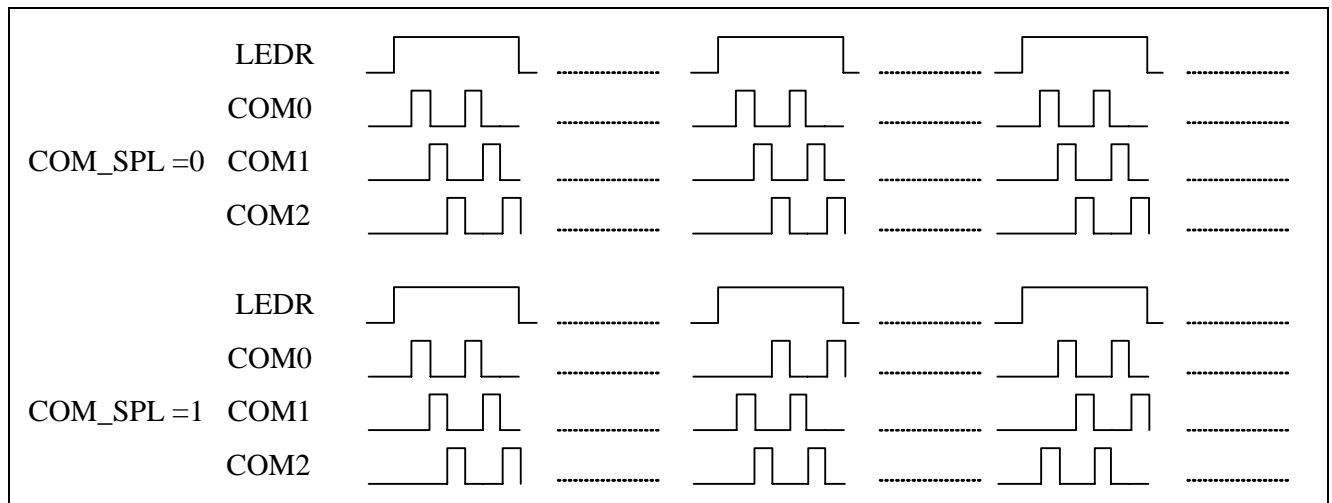


Figure 25: COM_SPL function

6.1.3. LCD Setup3

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
03H	LCD Setup3	0	0	PKSEL1	PKSEL0	0	CP_ON	OP_ON	OSC_ON	0000_0000

Bit	Function	Type	Description	Condition														
7	-	-	Reserved.															
6	-	-	Reserved.															
[5:4]	PKSEL	W	Charge pump clock select	<table border="1"> <thead> <tr> <th>PKSEL</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Pump clock = 3.75KHZ</td> </tr> <tr> <td>0</td> <td>1</td> <td>Pump clock = 7.5KHZ</td> </tr> <tr> <td>1</td> <td>0</td> <td>Pump clock = 15KHZ</td> </tr> <tr> <td>1</td> <td>1</td> <td>Pump clock = 30KHZ</td> </tr> </tbody> </table>	PKSEL	Function	0	0	Pump clock = 3.75KHZ	0	1	Pump clock = 7.5KHZ	1	0	Pump clock = 15KHZ	1	1	Pump clock = 30KHZ
PKSEL	Function																	
0	0	Pump clock = 3.75KHZ																
0	1	Pump clock = 7.5KHZ																
1	0	Pump clock = 15KHZ																
1	1	Pump clock = 30KHZ																
3	-	-	Reserved.															
2	CP_ON		Charge pump on	0= Charge pump off 1= Charge pump on														
1	OP_ON		LCD OP on	0= LCD OP (VLCD V2 V1) off 1= LCD OP (VLCD V2 V1) on														
0	OSC_ON		Oscillator on	0= Oscillator off 1= Oscillator on														

6.1.4. OSC TIME BASE

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
04H	OSC TIME BASE	0	0	0	0	0	OSCT2	OSCT1	OSCT0	0000_0000

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
5	-	-	Reserved.	
4	-	-	Reserved.	
3	-	-	Reserved.	
[2:0]	OSCT	-	OSC Time base. Please refer to 5.4.2.2. One Color field. LCDTxy / LCD time base = 120KHZ/ (OSCT+1)	

6.1.5. Blank Time

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
05H	Blank Time	BLPOL	COMRSEQ	COMLSEQ	BLT4	BLT3	BLT2	BLT1	BLT0	0000_0000

Bit	Function	Type	Description	Condition
7	BLPOL	W	Blank polarity	0= COM-SEG voltage is ground when blanking. 1= COM-SEG voltage is VLCD when blanking.
6	COMRSEQ	W	COMR sequence. Please refer to 5.2. Figure 19.	0 = COMR is normal order. 1 = COMR is reverse order.

Bit	Function	Type	Description	Condition
5	COMLSEQ	W	COML sequence. Please refer to 5.2. Figure 19.	0 = COML is normal order. 1 = COML is reverse order.
4:0]	BLT	W	Blanking time. Please refer to 5.5.2.2. Figure 23, Figure 24.	Blanking time = (BLT)*0.1ms

6.1.6. LCD Time Base x (x=0~3)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
06H	LCD Time Base0	0	0	0	LCDT04	LCDT03	LCDT02	LCDT01	LCDT00	0000_0000
07H	LCD Time Base1	0	0	0	LCDT14	LCDT13	LCDT12	LCDT11	LCDT10	0000_0000
08H	LCD Time Base2	0	0	0	LCDT24	LCDT23	LCDT22	LCDT21	LCDT20	0000_0000
09H	LCD Time Base3	0	0	0	LCDT34	LCDT33	LCDT32	LCDT31	LCDT30	0000_0000

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
5	-	-	Reserved.	
[4:0]	LCDTx	W	LCD time base in fieldx (x=0~3). LCDT0 defines time base in field0. LCDT1 defines time base in field1. Please refer to 5.5.2.1. One Figure 22 and 5.5.2.2. Figure 23, Figure 24.	$F_{com0} = F_{osc} / (OSCT + 1) / (LCDT0 + 16)$ $F_{com1} = F_{osc} / (OSCT + 1) / (LCDT1 + 16)$ $F_{com2} = F_{osc} / (OSCT + 1) / (LCDT2 + 16)$ $F_{com3} = F_{osc} / (OSCT + 1) / (LCDT3 + 16)$

6.1.7. LED Setup1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0AH	LED Setup1	0	0	LEDT5	LEDT4	LEDT3	LEDT2	LEDT1	LEDT0	0000_0000

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
[5:0]	LEDT	W	LED delay time. Please refer to 5.5.2.2. Figure 23, Figure 24.	LED delay time = (LEDT)*0.1ms

6.1.8. Field Setup x (x=0~3)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0BH	Field Setup0	ALLON0	ALLOFF0	0	0	0	B0	G0	R0	0000_0000
0CH	Field Setup1	ALLON1	ALLOFF1	0	0	0	B1	G1	R1	0000_0000
0DH	Field Setup2	ALLON2	ALLOFF2	0	0	0	B2	G2	R2	0000_0000
0EH	Field Setup3	ALLON3	ALLOFF3	0	0	0	B3	G3	R3	0000_0000

Bit	Function	Type	Description	Condition
7	ALLONx	W	ALLON in fieldx (x=0~3)	0 = normal LCD display in fieldx (x=0~3) 1 = LCD all on in fieldx (x=0~3)
6	ALLOFFx	W	ALLOFF in fieldx (x=0~3)	0 = normal LCD display in fieldx (x=0~3) 1 = LCD all off in fieldx (x=0~3)
5	-	-	Reserved.	

Bit	Function	Type	Description	Condition
4	-	-	Reserved.	
3	-	-	Reserved.	
2	Bx	W	Blue LED ON in fieldx (x=0~3)	0 = Blue LED OFF in fieldx (x=0~3) 1 = Blue LED ON in fieldx (x=0~3)
1	Gx	W	Green LED ON in fieldx (x=0~3)	0 = Green LED OFF in fieldx (x=0~3) 1 = Green LED ON in fieldx (x=0~3)
0	Rx	W	Red LED ON in fieldx (x=0~3)	0 = Red LED OFF in fieldx (x=0~3) 1 = Red LED ON in fieldx (x=0~3)

6.1.9. LED Setup2

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0FH	LED Setup2	LED_EN	LED_POL	0	0	0	LEDW	DRVSEL1	DRVSEL0	0000_0000

Bit	Function	Type	Description	Condition										
7	LED_EN	W	LED enable control	0 = R G B LED output tri-state 1 = R G B LED output active										
6	LED_POL	-	LED polarity	0 = LED output active high 1 = LED output active low										
5	-	-	Reserved.											
4	-	-	Reserved.											
3	-	-	Reserved.											
2	LEDW	W	LED white	0 = R G B LED all off (output dark) in LED delay time 1 = R G B LED all on (output white) in LED delay time										
[1:0]	DRVSEL	W	LED output driving strength	<table border="1"> <thead> <tr> <th>DRVSEL</th> <th>LED output driving strength</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>0.5mA</td> </tr> <tr> <td>0 1</td> <td>1mA</td> </tr> <tr> <td>1 0</td> <td>2mA</td> </tr> <tr> <td>1 1</td> <td>4mA</td> </tr> </tbody> </table>	DRVSEL	LED output driving strength	0 0	0.5mA	0 1	1mA	1 0	2mA	1 1	4mA
DRVSEL	LED output driving strength													
0 0	0.5mA													
0 1	1mA													
1 0	2mA													
1 1	4mA													

6.1.10. LED status

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
10H	LED status	0	0	0	0	0	0	LEDS(R)	LEDS(R)	

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
5	-	-	Reserved.	
4	-	-	Reserved.	
3	-	-	Reserved.	
2	-	-	Reserved.	
[1:0]	LEDS	R	Field status. Show the current field number.	

6.1.11. Software reset

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
13H	Software reset	Write A5'H to implement Soft reset								

6.1.12. MAX Field number

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
14H	MAX Field number	0	0	0	0	0	MXFLD2	MXFLD1	MXFLD0	0000_0000

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
5	-	-	Reserved.	
4	-	-	Reserved.	
3	-	-	Reserved.	
[2:0]	MXFLD	W	Max plane number. Please refer to 5.5.2.1. Figure 22.	Max plane = MXFLD + 1

6.1.13. Field control

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
15H	Field control	0	FLDNM2	FLDNM1	FLDNM0	0	0	FLDSEL1	FLDSEL0	xxxx_xxxx

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
[6:4]	FLDNM	W	Plane number	
3	-	-	Reserved.	
2	-	-	Reserved.	
[1:0]	FLDSEL	W	Field select	

Please refer to 5.4.2.1. Figure 22. There are 8 planes in one LCD frame at most. There are 4 field settings. Each plane corresponds to one field settings in four.

For example, there are eight planes in one LCD frame (MXFLD = 07'H). It is set plane0 as field1, plane1 as field0, plane2 as field3, plane3 as field2, plane4 as field0, plane5 as field1, plane6 as field2, and plane2 as field3.

Users should write 01'H to Field Control (15'H). (Plane number = 0, field select = 1, which is plane0 as field1.)

10'H to Field Control (15'H). (Plane number = 1, field select = 0, which is plane1 as field0.)

23'H to Field Control (15'H). (Plane number = 2, field select = 3, which is plane2 as field3.)

32'H to Field Control (15'H). (Plane number = 3, field select = 2, which is plane3 as field2.)

40'H to Field Control (15'H). (Plane number = 4, field select = 0, which is plane4 as field0.)

51'H to Field Control (15'H). (Plane number = 5, field select = 1, which is plane5 as field1.)

62'H to Field Control (15'H). (Plane number = 6, field select = 2, which is plane6 as field2.)

73'H to Field Control (15'H). (Plane number = 7, field select = 3, which is plane7 as field3.)

Notes: If MXFLD max plane number is not 7, the first unused plane should be set as the first plane (plane number 0).

For example, when MXFLD is 2, there are 3 planes in one LCD frame.

And plane0 is set as field1. The first unused plane (plane3) should be set as field1 (the same as plane0).

6.1.14. RAM dummy address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
16H	RAM dummy address									

This register is only used for I²C RAM read-modify-write function. In RAM read-modify-write mode, RAM address will auto increment after writing data to RAM. However, in I²C mode, register address should be sent whenever writing data to RAM. When

RAM dummy address (16'H) is sent to GPLD94160, RAM address will auto increment in spite of RAM dummy address. Please refer to Read-Modify-Write RAM data figure (Figure 18) in 5.1.2.3 Serial Interface (I²C Interface).

6.1.15. RAM control

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
17H	RAM control	0	0	0	0	0	0	RMW	RGB	0000 0000

Bit	Function	Type	Description	Condition
7	-	-	Reserved.	
6	-	-	Reserved.	
5	-	-	Reserved.	
4	-	-	Reserved.	
3	-	-	Reserved.	
2	-	-	Reserved.	
1	RMW	W	Read-Modify-Write Mode	0 = Disable Read-Modify-Write Mode 1 = Enable Read-Modify-Write Mode
0	RGB	W	RGB mode. Please refer to 5.2.1.1. DDRAM sequential read/write.	0 = Pixel mode 1 = Color field mode

6.1.16. Line data start address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
18H	Line data start address	0	0	0	0	0	0	LNSADR1	LNSADR0	0000 0000

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 19, Figure 20).

6.1.17. Line data end address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
19H	Line data end address	0	0	0	0	0	0	LNEADR1	LNEADR0	0000 0011

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 19, Figure 20).

6.1.18. COM display data start line

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
1AH	COM display data start line	0	0	0	0	0	0	CDSLIN1	CDSLIN0	0000 0000

This COM display data start line corresponds to the first line (COM0) of the display. Therefore, by setting COM display data start line repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM.

For 2-COM or 1-COM application, by setting COM display data start line, LCD display RAM area can be different from the RAM area is written to. Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 19, Figure 20).

6.1.19. SEG data start address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
1CH	SEG data start address	0	0	1	SSADR4	SSADR3	SSADR2	SSADR1	SSADR0	0010_0000

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 20, Figure 21).

6.1.20. SEG data end address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
1DH	SEG data end address	0	0	1	SEADR4	SEADR3	SEADR2	SEADR1	SEADR0	0011_1111

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 20, Figure 21).

6.1.21. Color field start address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
1EH	Color field start address	0	0	0	0	0	0	FDSADR1	FDSADR0	0000_0000

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 20, Figure 21).

6.1.22. Color field end address

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
1FH	Color field end address	0	0	0	0	0	0	FDEADR1	FDEADR0	0000_0011

Please refer to 5.2.1.1. DDRAM sequential read/write figure (Figure 20, Figure 21).

6.1.23. RAM data (SEG data)

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
20H~33H	RAM data (SEG data)	RAM data (SEG data)								xxxx_xxxx

Please refer to 5.2.DISPLAY DATA RAM (DDRAM) figure (Figure 19).

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply Voltage (1)	VDD	$T_A = +25^\circ\text{C}$ Referenced to VSS (0V)	VDD	-0.3 to +3.6	V
Supply Voltage (2)	V_0		V_{LCD}	-0.3 to +7.2	V
	V_1		V_1	-0.3 to $V_0 + 0.3$	V
	V_2		V_2	-0.3 to $V_0 + 0.3$	V
Input Voltage	V_I		LCDEN, MODE, SERI, CS, RD, WR, A0, DB[7:0], CK, FP, CHIPMODE	-0.3 to VDD + 0.3	V
Storage Temperature	T_{STG}	-	-	-50 to + 150	$^\circ\text{C}$

Note1: $T_A = +25^\circ\text{C}$

Note2: The maximum applicable voltage on any pin with respect to VSS (0V).

Note3: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

8.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Supply Voltage (1)	VDD	Referenced to VSS (0V)	VDD	+2.4	-	+3.6	V
Supply Voltage (2)	V_{LCD}		V_{LCD}	+3.45	-	+7.2	V
Operating Temperature	T_{OPR}	-	-	-20	-	+75	$^\circ\text{C}$

Note1: The applicable voltage on any pin with respect to VSS (0V).

8.3. DC Characteristics

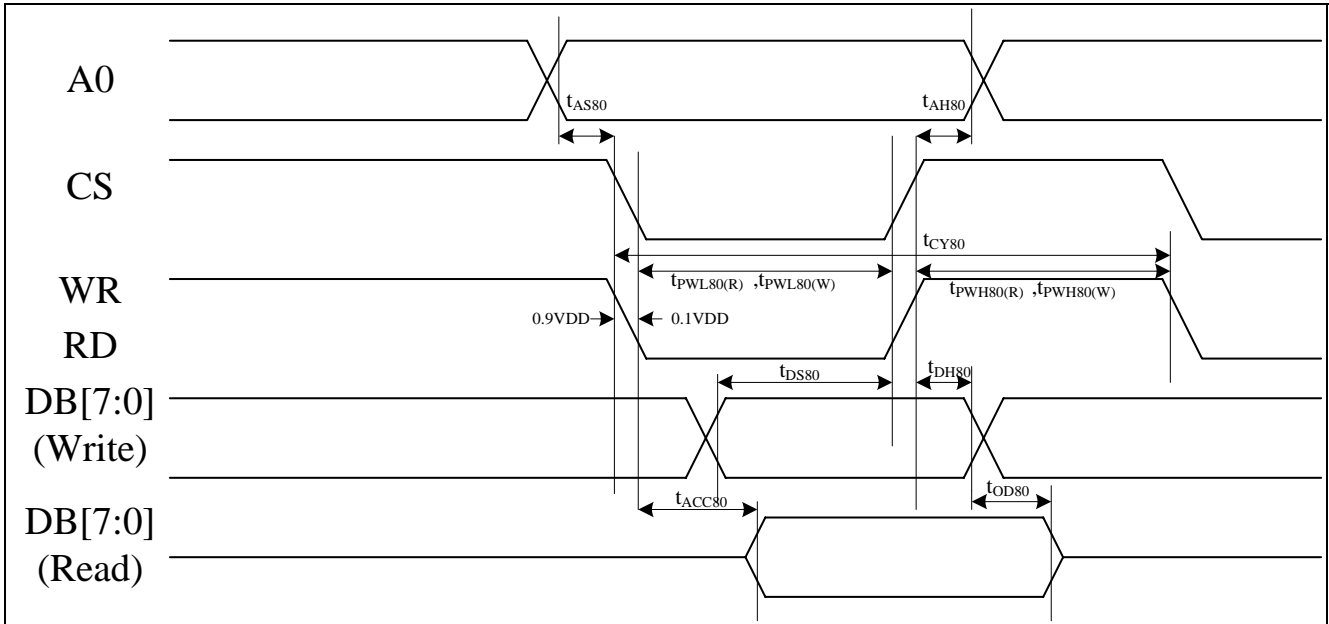
Parameter	Symbol	Conditions	Applicable Pins	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	-	LCDEN, MODE, SERI, CS, RD, WR, A0, DB[7:0], CK, FP, CHIPMODE	0.8VDD	-	-	V
	V_{IL}	-		-	-	0.2VDD	V
Output Voltage	V_{OH}	$I_{OH} = -0.4\text{mA}$	DB[7:0], CK, FP	VDD - 0.4	-	-	V
	V_{OL}	$I_{OL} = +0.4\text{mA}$		-	-	+0.4	V
Output Voltage (LED output)	V_{LOH}	$I_{OH} = -4\text{mA}$ (DRVSEL=11'B)	LEDR, LEDG, LEDB	VDD - 0.7	-	-	V
	V_{LOL}	$I_{OL} = 4\text{mA}$ (DRVSEL=11'B)		-	-	0.7	V
Input Leakage Current	I_{LIH}	$V_I = VDD$	LCDEN, MODE, SERI, CS, RD, WR, A0, CHIPMODE	-	-	+1.0	μA
	I_{LIL}	$V_I = VSS$		-	-	-1.0	μA
Output Resistance	R_{ON}	$ \Delta V_{ON} = 0.5\text{V}$ $V_0 = +6.4\text{V}$	COMR[3:0], COML[3:0], SEG[159:0]	-	1.0	2.0	$\text{K}\Omega$
Oscillator Frequency	F_{OSC}	VDD=3V		-	120	-	KHZ
Voltage Converter Output Voltage	VPP		VPP	-	8	-	V
Voltage Follower Operating Voltage	VLCD		VLCD	3.45	-	7.2	V
Stand-by Current	I_{STB}	*1	VSS	-	-	1.0	μA
Supply Current (1)	I_0	*2	VLCD	-	-	90	μA

Note1: VDD = +3.0V, LCDEN pin = "L".

Note2: VDD = +3.0V, VLCD= +7.2V, $f_{CK} = 120\text{KHz}$, Frame Rate= 140HZ. LED off.No-load

8.4. AC Characteristics

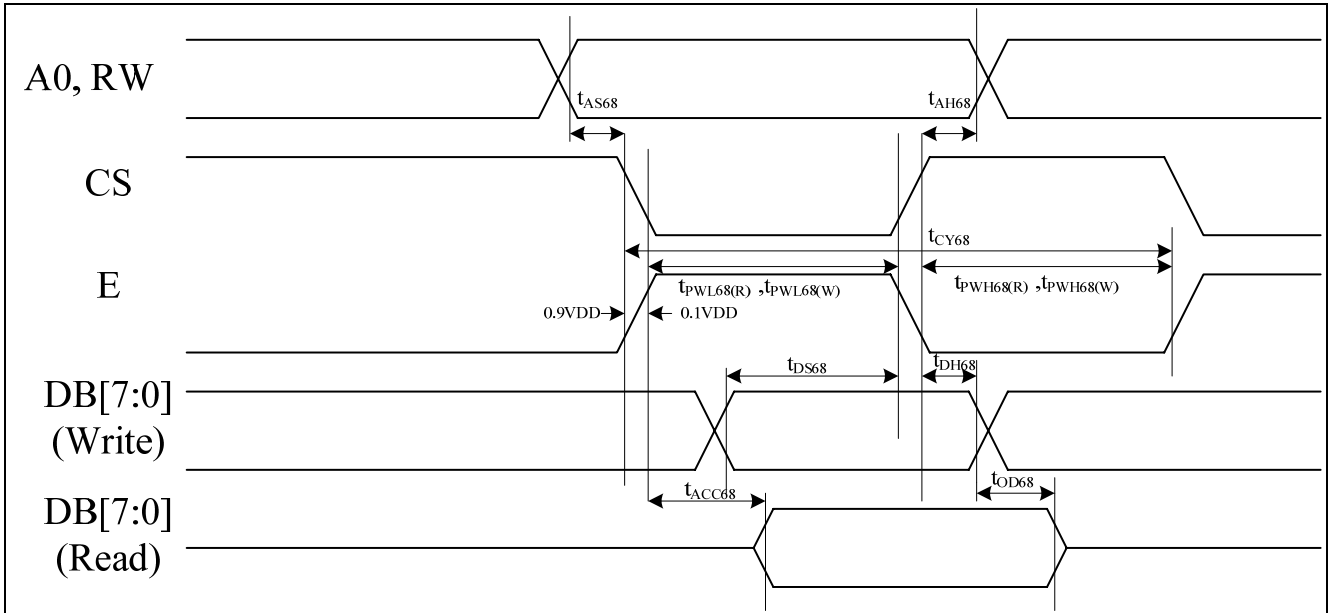
8.4.1. Read / Write Characteristics (8080-series MPU)



Read / Write Characteristics (8080-series MPU) (VDD = 2.4 to 3.6V, Ta = 25°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark	
Address setup time	A0	tAS80	0	-	-	ns		
Address hold time		tAH80	0	-	-	ns		
System cycle time	WR RD	tCYC80	150	-	-	ns		
Enable Pulse Low width	Read	RD	tPWL80 (R)	70	-	-	ns	
	Write	WR	tPWL80 (W)	70	-	-	ns	
Enable Pulse High width	Read	RD	tPWH80 (R)	70	-	-	ns	
	Write	WR	tPWH80 (W)	70	-	-	ns	
Data setup time	DB7 to DB0	tDS80	20	-	-	ns		
Data hold time		tDH80	5	-	-	ns		
Read access time		tACC80	-	-	30	ns	CL=30p	
Output disable time		tOD80	-	-	30	ns		

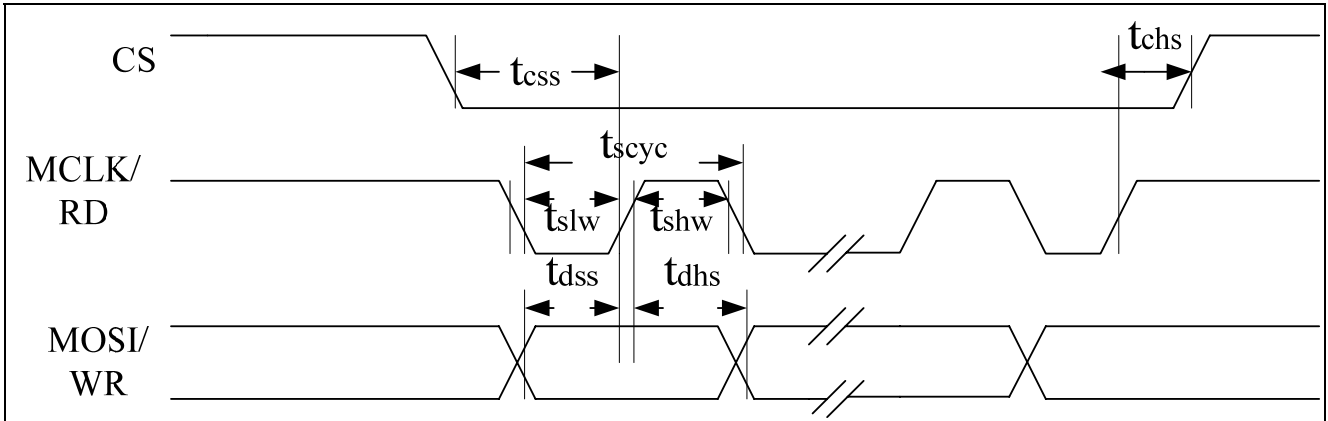
8.4.2. Read / Write Characteristics (6800-series Microprocessor)



Read / Write Characteristics (6800-series Microprocessor) (VDD = 2.4 to 3.6V, Ta = 25°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time	A0, RW	tAS68	0	-	-	ns	
Address hold time		tAH68	0	-	-	ns	
System cycle time	E	tCYC68	150	-	-	ns	
Enable Pulse Low width	Read	tPWL68 (R)	70	-	-	ns	
	Write	tPWL68 (W)	70	-	-	ns	
Enable Pulse High width	Read	tPWH68 (R)	70	-	-	ns	
	Write	tPWH68 (W)	70	-	-	ns	
Data setup time	DB7 to DB0	tDS68	20	-	-	ns	
Data hold time		tDH68	5	-	-	ns	
Read access time		tACC68	-	-	30	ns	
Output disable time		tOD68	-	-	30	ns	CL=30p

8.4.3. Serial Interface Characteristics



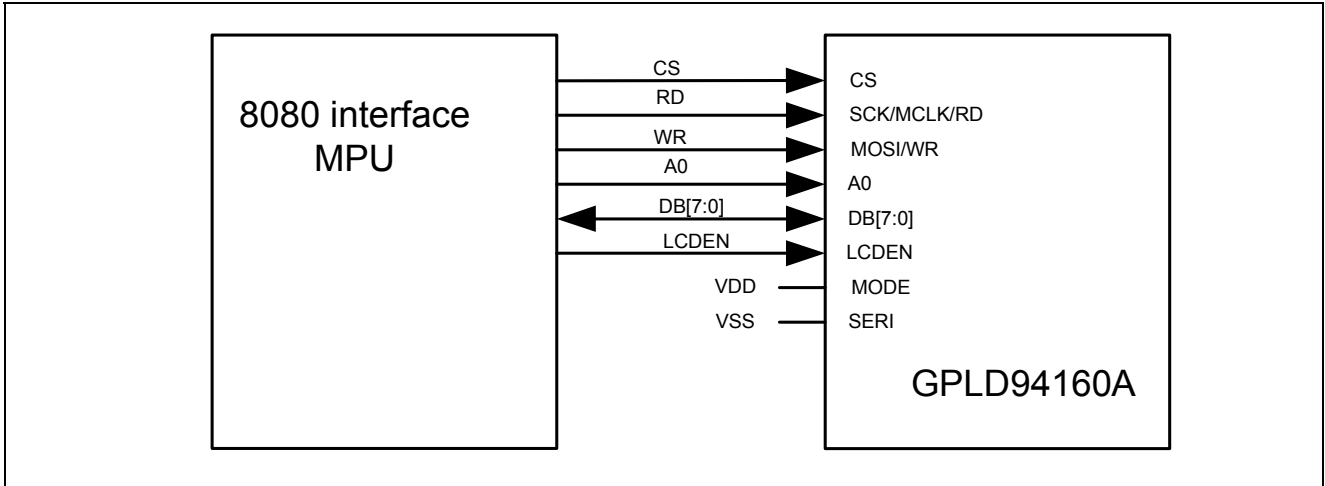
Serial Interface Characteristics (VDD = 2.4 to 3.6V, Ta = 25°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	MCLK /RD	tCYS	90				
SCLK high pulse width		tWHS	40	-	-	ns	
SCLK low pulse width		tWLS	40				
Data setup time	MOSI /WR	tDSS	40	-	-	ns	
Data hold time		tDHS	40				
CS setup time	CS	tCSS	40	-	-	ns	
CS hold time		tCHS	40				

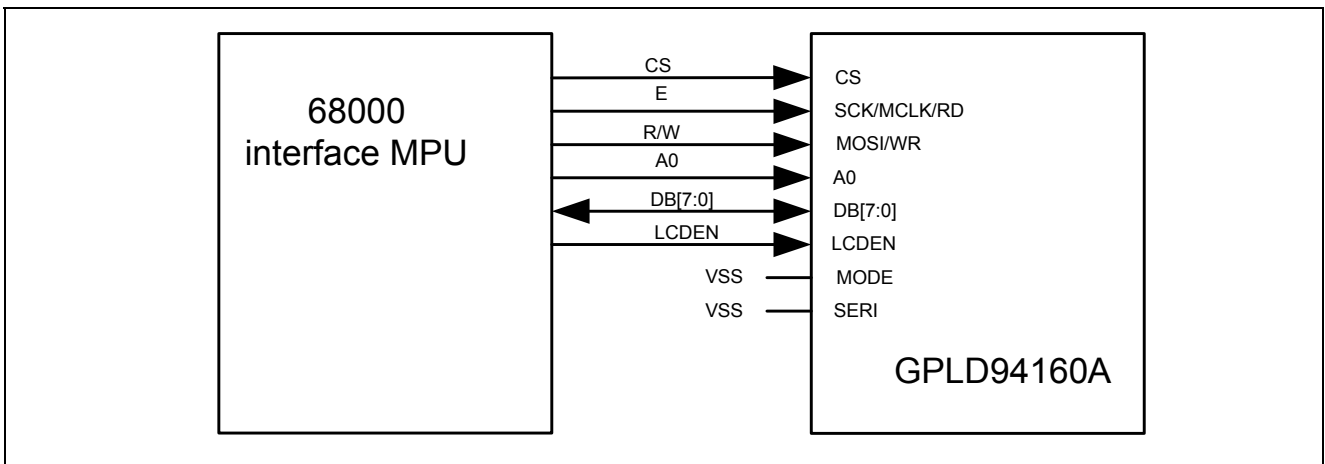
9. APPLICATION CIRCUITS

9.1. Microprocessor Interface

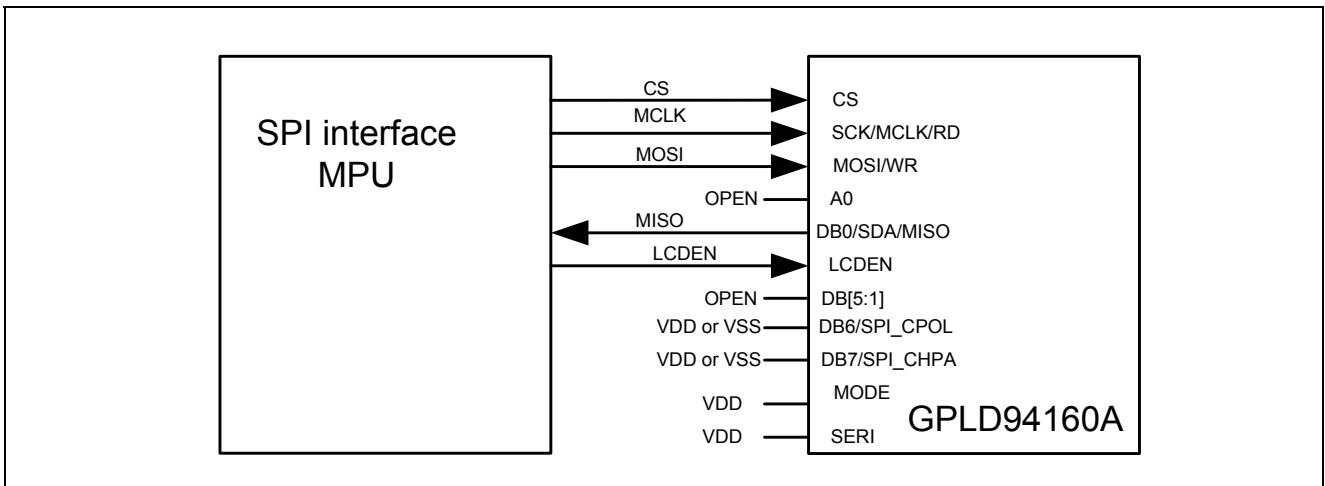
9.1.1. 8080 interface



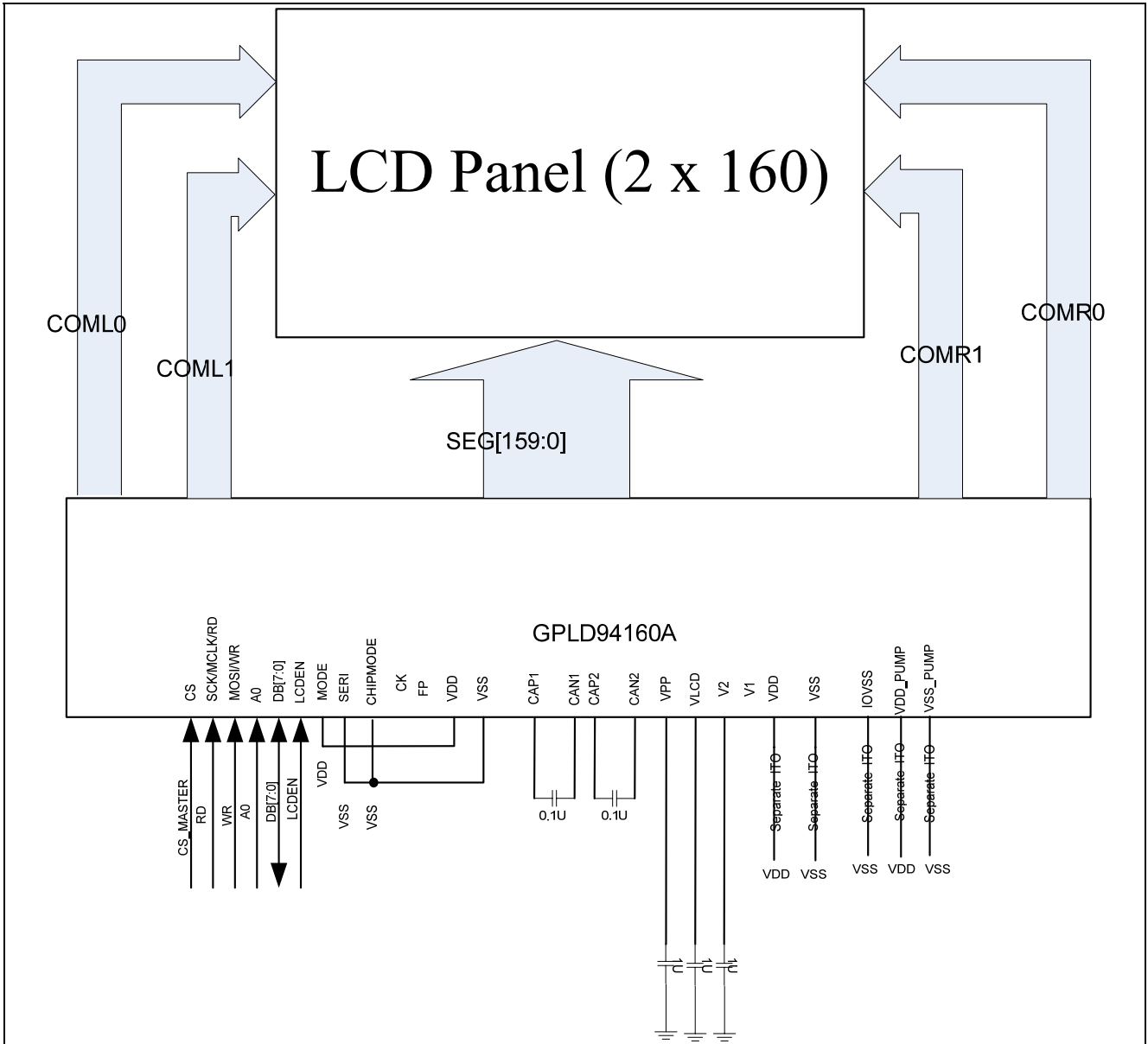
9.1.2. 68000 interface



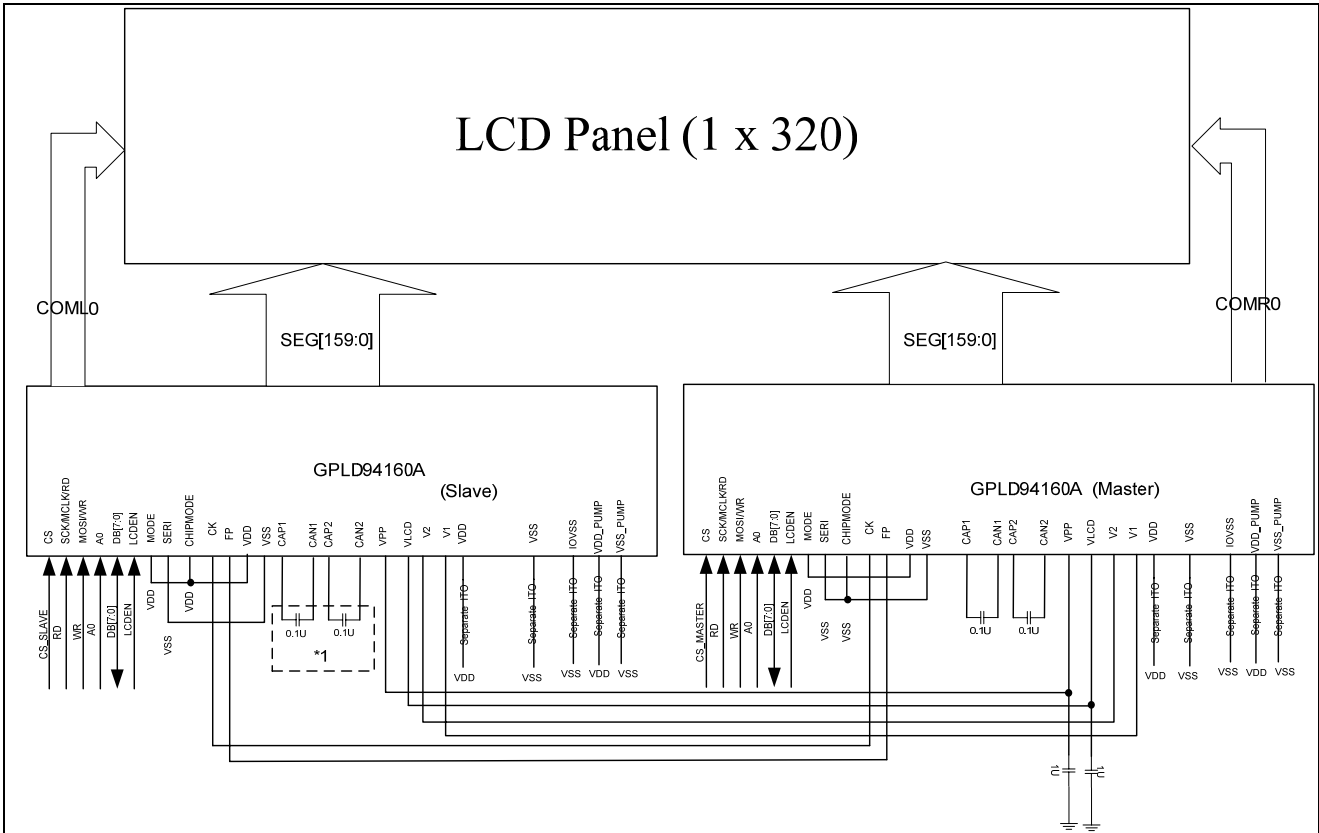
9.1.3. SPI interface



9.3. Master LCD Driver, 2 Commons x 160 Segments, 1/2 bias



9.4. Master and Slave LCD Drivers, 1 Common x 320 Segments, Static



Note*1: These capacitors on slave chip can be removed if the LCD panel loading is small and VLCD voltage does not drop. If not, the charge pump circuit in slave chip should be turned on to hold VLCD voltage.

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPLD94160A-NnnV-C	Chip Form with Gold Bump

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
Aug. 5, 2009	1.0	<ol style="list-style-type: none"> 1. Add Recommended I/O PIN ITO Resistance 2. Fix Figure 2, 4, 5 error 3. Fix Figure 13 error 4. Fix pixel mode error 5. Modify 6.1.13 Field control 6. Modify 8.2.Recommended Operating Conditions 7. Modify 8.3.DC Characteristics 8. Add 8.4. AC Characteristics 	<p>8</p> <p>10-11</p> <p>14</p> <p>17</p> <p>28</p> <p>32</p> <p>32</p> <p>33</p>
Jun. 3, 2009	0.2	<ol style="list-style-type: none"> 1. Change COMR3~COMR0 COML3~COML0 pad locations and pad assignment 2. Fix Figure 9 error 3. Modify application circuit in 9.2 9.3 9.4. 	<p>7, 9</p> <p>13</p> <p>34-36</p>
Mar. 17, 2009	0.1	Preliminary data sheet	39